

Modular Power Electronic Converters in the Power Range 1 to 10 kW

by

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Abstract

Thanks to CO₂ emission reduction policies and increasing prices of fossil fuels a significant growth in field of sustainable energy sources (SES) is being observed during last decade. A government support and take-off projects in Europe and US shall ensure an increasing trend in future too. Some of SES based plants, like hydro-, geothermal-, biofuel-plants, use synchronous generators directly connected to the grid. But some other SES technologies, like fuel cell or photovoltaic, require a power electronic converter between the energy source and the load or the grid. Work presented in this thesis concentrates on dc-dc non-isolated converters suitable for high voltage gain applications, like uninterruptible power supply (UPS) and some of sustainable energy sources. A special attention is on reduction of power losses and efficiency improvements in non-isolated dc-dc step-up converters.

During literature study many different non-isolated dc-dc step-up topologies were found, however not all of them are desired for high voltage gain applications. It's found that converters based on an inductor and a coupled-inductor principle (a boost and a center tapped boost converters) as well as converters derived from isolated converters (a non-isolated flyback-boost, a non-isolated push-pull-boost and a non-isolated two-inductor-boost converters) are good candidates for future investigation. Analysis and comparison of selected, most promising topologies indicated that a non-isolated push-pull-boost and a non-isolated two-inductor-boost converters are the best candidates for applications requiring a high voltage gain.

Design of a high efficiency converter requires a detailed knowledge and accurate prediction of power losses. For this purpose average steady-state models of selected topologies and component loss models are developed and implemented in MATLAB. Converter models base on analysis of ideal waveforms and are built-up from set of equations describing values essential for power loss calculation, e.g. average or rms current values. These data are used by component models to calculate losses in particular components. It's important that component models use parameters from datasheets in most cases. It enables performance comparison of different topologies as well as comparison of different components. The proposed modeling approach was verified using a basic boost converter breadboard. With small modification these models may be used for design purposes, like search for optimum output power and optimum switching frequency for given topology and given MOSFETs.

Using developed tools and models the converter breadboard was designed. The breadboard demonstrated a very high efficiency, comparable with present state-of-the-art isolated converters.

A modular converter concept and its influence on a fuel cell converter overall efficiency were investigated too. Based on simulation and measurement results it

was demonstrated that the parallel modular converter used in a fuel cell application achieves a high efficiency over wide range of the output power. Moreover, the efficiency increases while the output power decreases, which is opposite to a solid converter solution.

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Abbreviations and Symbols

Abbreviations

CCM	continuous conduction mode
DCM	discontinuous conduction mode
ESR	equivalent series resistance of a capacitor
FC	fuel cell
FEM	finite element method
FOM	figure of merit
HV	high voltage (about the output voltage)
IC	integrated circuit
IGBT	insulated gate bipolar transistor
LV	low voltage (significantly lower than the output voltage)
MOSFET	metal-oxide semiconductor field-effect transistor
PV	photovoltaic source
SES	sustainable energy source(s)
SVS	switched voltage source inverter
UPS	uninterruptible power source
VHV	very high voltage (significantly higher than the output voltage)

Style of writing

i or $i(t)$, etc.	instantaneous values
$I_{(\text{rms})}$, etc.	rms values of ac and dc components
I , etc.	average, dc values
$I_{(\text{ac})}$, etc.	rms values of ac component
$I_{(\text{pp})}$, etc.	peak-to-peak values
Δi , etc.	amplitude values

Symbols

<i>Symbol</i>	<i>Description</i>	<i>Unit</i>
A	area	m^2
AP	area product values of magnetic core	m^4

B	flux density, flux density	T
C	capacitance	F
D	transistor duty cycle	%
δ	penetration depth	m
f_{eq}	equivalent frequency	Hz
f_r	repetition frequency	Hz
f_s	switching frequency	Hz
F_R	ac to dc resistance factor	-
Φ	magnetic flux	Wb
g_{fm}	transistor forward transconductance	S
h	layer thickness	m
i, I	current	A
I_C	capacitor current	A
I_D	diode current	A
I_{in}	input current	A
I_L	inductor current	A
I_{out}	output current	A
I_T	transistor current	A
l	length	m
L	inductance	H
L_M	magnetizing inductance	H
λ	volt-seconds applied to the winding	V·s
M	voltage gain or number of layers	-
μ	permeability	H/m
n	turns ratio, number of turns (inductor)	-
n_1, n_2	number of turns (transformer)	-
N	number of phases	-
η	efficiency or porosity factor	%
p_{Fe}	specific core loss (per volume unit)	W/m ³
P	power or power loss	W
P_C	capacitor loss	W
P_{Cuac}	ac copper loss	W
P_{Cude}	dc copper loss	W
P_{Dcap}	diode capacitive loss	W
P_{Dcond}	diode conduction loss	W
P_{Doff}	diode turn-off loss	W
P_{Don}	diode turn-on loss	W
P_{Fe}	core loss	W

P_{in}	input power	W
P_{out}	output power	W
P_{Tcond}	transistor conduction loss	W
P_{Tgate}	transistor gate drive loss	W
P_{Trr}	loss due to diode reverse recovery	W
P_{Tsw}	transistor switching loss	W
Q	charge	C
Q_{G}	gate charge	C
Q_{rr}	reverse recovery charge	C
R	resistance	Ω
$r_{\text{DS(on)T}}$	on-state resistance temperature coefficient	$\Omega/^{\circ}\text{C}$
r_{FT}	forward resistance temperature coefficient of diode	$\Omega/^{\circ}\text{C}$
$R_{\text{DS(on)}}$	transistor on-state resistance	Ω
$R_{\text{DS(on)25}}$	transistor on-state resistance at 25 $^{\circ}\text{C}$	Ω
R_{F}	diode forward resistance	Ω
R_{F25}	diode forward resistance at 25 $^{\circ}\text{C}$	Ω
R_{L1}	inductor winding resistance	Ω
R_{n}	transformer winding resistance	Ω
ρ	resistivity	$\Omega\cdot\text{m}$
t	time	s
t_{if}	current fall time	s
t_{ir}	current rise time	s
t_{vf}	voltage fall time	s
t_{vr}	voltage rise time	s
T	temperature or time period	$^{\circ}\text{C}$, s
T_{j}	junction temperature	$^{\circ}\text{C}$
W	energy or energy loss	J
v, V	voltage	V
v_{DT}	forward voltage temperature coefficient of diode	$\text{V}/^{\circ}\text{C}$
V_{GS}	gate-source voltage	V
V_{D}	diode anode-cathode voltage	V
$V_{\text{D(F)}}$	diode forward voltage (for loss calculation)	V
$V_{\text{D(R)}}$	diode reverse voltage	V
V_{in}	input voltage	V
V_{n}	winding voltage	V
V_{out}	output voltage	V
V_{T}	transistor drain-source voltage	V
$V_{\text{T(off)}}$	transistor blocking voltage	

Chapter 1

Introduction

Work presented in this thesis concentrates on dc-dc non-isolated converters suitable for high voltage gain applications, like uninterruptible power supply (UPS) or some of sustainable energy sources (SES). Three main issues are presented. First, state-of-the-art in dc-dc non-isolated step-up converters is presented. Several topologies are presented, its features are discussed in general and the most promising solutions are selected for further investigation. An overview on power loss distribution in relation to presented topologies is given too. Second, the most promising topology is chosen. The converter breadboard is being designed, optimized and built. Laboratory tests are performed to verify its performance and efficiency. Finally, parallel operation of multiple dc-dc modules is investigated. It includes interaction between modules and a controller, optimum utilization of a single module and final tests.

First, this chapter will discuss background for the research work made in this thesis. It includes introduction to and discussion on possible applications and issues related to a non-isolated grid connected system. Next, the initial problem is defined and preliminary limitations are specified. The outline of the thesis and the list of publications are presented at the end of this chapter.

1.1 Background and motivation

Thanks to CO₂ emission reduction policies and increasing prices of fossil fuels a significant growth in field of sustainable energy is being observed during last decade. A government support and take-off projects in Europe and US shall ensure an increasing trend in future too [1, 2]. SES is a wide term and it covers all renewable energy sources such as biofuels, solar power, wind power, wave power and geothermal power. Hydrogen power and sometimes nuclear power are considered as SES too. Some of SES based power plants, including hydro-, geothermal-, biofuel-plants, use synchronous generators directly connected to the grid. But some other sources like fuel cells (FC) and photovoltaic (PV) basically produce a dc voltage which has to be converted to an ac voltage suitable for the grid. So, an interface between the source and the grid is a need and the power electronic converter is the interface.

This project, entitled “Modular power electronic converters in the power range 1 to 10 kW”, is being realized in cooperation between Aalborg University, Danmarks Tekniske Universitet and companies: Grundfos Management A/S, KK-Electronic

A/S, IRD Fuel Cell Technology A/S and Danfoss Solar Inverters A/S (former PowerLynx A/S). Each of these companies has interest in development and implementation of highly efficient power electronic converter, which converts a low dc voltage to 50/60 Hz ac voltage required by utility grid or commercial loads. The converter like this will be suitable for sustainable energy sources, like fuel cells and photovoltaic and for UPS systems in the power range from few kilowatts to tens of kilowatts.

1.2 Potential applications

This project focuses on high voltage gain applications in which a step-up dc-dc converter must be used. It includes sustainable energy, especially fuel cells and photovoltaic as well as battery based UPS systems. This section will present general aspects of these applications.

1.2.1 Fuel cell

In the simplest words a fuel cell is an electrochemical device which converts chemical energy of a fuel and an oxidant directly into electrical energy and heat available for users. Basically all fuel cells operate on the same principle, however they use different electrolytes materials. Most recognized kinds of fuel cells are: proton-exchange membrane fuel cell (PEMFC), alkaline fuel cell (AFC), phosphoric acid fuel cell (PAFC), molten carbonate fuel cell (MCFC), solid oxide fuel cell (SOFC) and direct methanol fuel cell (DMFC). Another classification bases on the operating temperature of a fuel cell. Low temperature fuel cells operate below 200°C and are suitable for portable and automotive applications and for low power co-generation. Medium temperature fuel cells operate between 200°C and 600°C and can be used for automotive applications and co-generation including combined heat and power (CHP). Finally high temperature fuel cells operate above 600°C and the main application is CHP plants in the power range up to hundreds of kilowatts. The no-load voltage of a single cell is limited to 1.23 V in an ideal case, but in practice it's about 1 V for hydrogen fuel. During normal operation the voltage drops down to 0.7-0.5 V. To increase the output voltage cells are connected in series and forms fuel cell stack. Due to practical problems related to the cell voltage balancing and fuel/oxidant distribution limit number of series connected cells and the stack output voltage [3, 4].

The fuel cell market is just growing. The major barriers for wide spread use of fuel cells are a high cost, a short lifetime of a fuel cell and lack of a pure hydrogen fuel. However a significant growth is predicted in next years. In Europe it's expected to install fuel cell plants with total power of 1 GW before 2015 [5, 6].

Nowadays there are several commercially available fuel cells. Most of them are a low temperature PEMFC with the output power from few hundred watts up to few kilowatts. The output voltage of such fuel cell usually is somewhere between 12-60 V.

1.2.2 Photovoltaic

Photovoltaic cells are usually known as 'solar cells'. Photovoltaic cells work by transforming the photon energy from solar radiation directly into electrical energy without an intermediate mechanical process. There are many inorganic and organic materials used to manufacture photovoltaic cells. The most spread however is silicon [7]. Based on silicon crystal structure there are mono-crystalline cells, poly-crystalline cells and thin-film (amorphous) cells. Among them mono-crystalline PVs provide the highest efficiency, but they are the most expensive. On the other end there are thin-film PVs which are fairly cheap, but have worse performance. A single PV cell delivers the voltage up to 0.6 V at no-load conditions. To increase the output voltage single cells are connected in series and forms PV panels. Often panels are connected in series and forms PV strings [8].

Contrary to the fuel cell market, the PV market is well developed and it's growing fast. In 2008 there was about 15 GW of photovoltaic power installed worldwide [9]. The same analysis predicts new PV plants with total power of 22 GW in 2013. Current research projects are primarily focused on cost reduction [1].

There are many PV panels manufacturers around the world. Most of commercial PV panels have the output power in the range of 100-400 W and the output voltage about 20-45 V (per single panel). To increase the power or the voltage level panels are connected and they form strings and arrays.

1.2.3 Uninterruptible power supply

Uninterruptible power supply (UPS) is a device providing an emergency power when grid is not available. UPS are primarily used for power back-up of: computers, servers, telecom equipment and medical equipment. The output power of UPS varies from few hundred volt-amps to megavolt-amps and the back-up time vary from seconds to hours. UPS based on lead-acid batteries can deliver power up to tens of kilovolt-amps and back-up time from few minutes up to few hours. A high power battery based UPS usually incorporates so called double conversion. Because of a high voltage battery banks used in such UPS there is no need for high step-up voltage conversion. This solution provides the best protection but it's the most expensive one. Many of commercial low power UPS products are so called off-line or standby UPS. These products usually have a single 12 V or 24 V lead-acid battery, thus there is an obvious need for a high step-up conversion. UPS application however creates one more challenge for a power converter. Contrary to a fuel cell or a photovoltaic cell, a battery is a rechargeable source, which requires bidirectional power flow. Bidirectional power flow in low power off-line UPS is ensured in two ways – by use of a bidirectional converters or by use of a dedicated battery charger next to the main converter.

1.3 Overview on a non-isolated system

Lack of an isolation between an input and an output of the non-isolated power conversion system creates certain issues. One of the most important questions is about a source grounding?

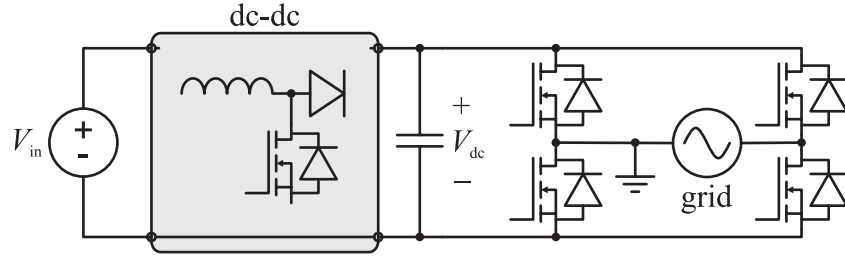


Figure 1.1 A non-isolated power conversion system with a full-bridge inverter

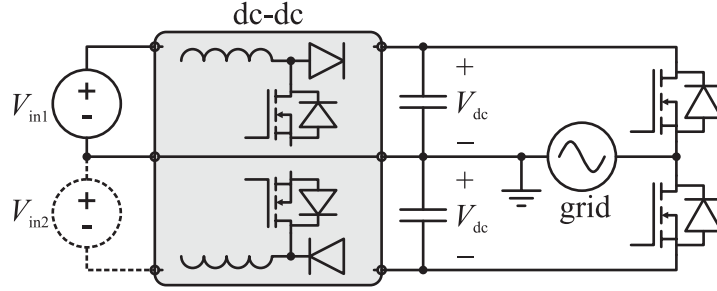


Figure 1.2 A non-isolated power conversion system with a half-bridge inverter

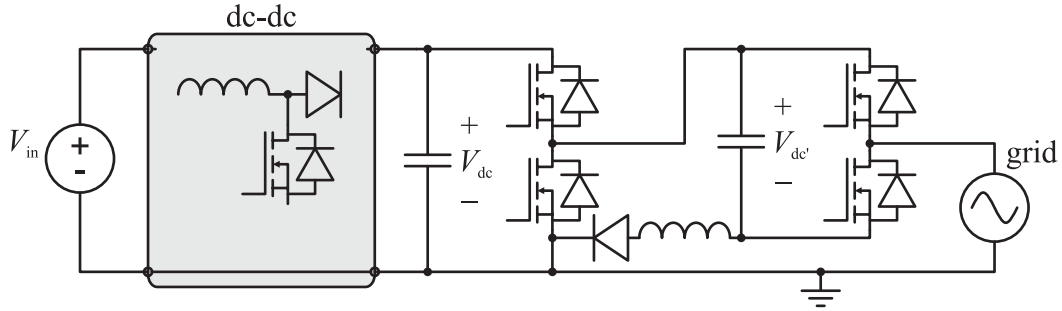


Figure 1.3 A non-isolated power conversion system with a SVS inverter

Figure 1.1 presents a non-isolated converter with a full-bridge grid connected inverter. The source cannot be grounded in this case and it floats. Terminals of the source may jump between positive and negative potential of hundred volts with a high frequency. Usually it's not a problem if the source is a battery pack in an isolated enclosure. In case of floating PV panel one has to take care about ground leakage current, especially in case of a large PV arrays. Proper grounding of a PV panel terminal may reduce leakage ground current [10, 11]. Moreover such grounding is required in some countries (e.g. in USA) [11-13].

If grounding of a source terminal is required usually the first choice would be a system similar to the one presented on Figure 1.2. A half-bridge inverter is used and the source has a solid connection with neutral point of the grid, which usually is grounded in a load center [12, 13]. The main drawback of this solution is need for twice dc-link voltage compared with the full-bridge inverter based configuration. One way is to use of two series connected sources V_{in1} and V_{in2} together with two independent dc-dc converters for each dc-link voltage. If only a single source V_{in1} is available then an inverting converter (buck-boost) or a dual-output converter is

required [14-16]. A simple single-input dual-output step-up converter is presented and discussed in Appendix A, paragraph A.1. Use of two sources will increase cost of the whole system on one hand. On the other use of a single source requires a higher voltage gain which turns into efficiency degradation and more complex converter.

A power conditioning system with the switched voltage source (SVS) inverter presented on Figure 1.3 may solve problems addressed above [17]. Such configuration provides a solid connection between the source terminal and the grid neutral wire. In the same time the SVS inverter requires the same dc-link voltage like the full-bridge inverter. Reference [11] presents another single-stage non-isolated power converters for systems with a grounded source.

1.4 Problem definition

Nowadays there are many different converter topologies and selection of the most suitable one is not straightforward choice. Such selection is a difficult trade off between converter's complexity, estimated cost, size and weight, power level and expected efficiency.

The goal of this project is to investigate features of different non-isolated dc-dc step-up converters dedicated for fuel cell application and suitable for other high voltage gain applications.

The aims of this project can be covered by the following statements:

- Can a non-isolated dc-dc converter work in a high voltage gain application as well as an isolated transformer based converter do?
- Which non-isolated dc-dc topology is the best candidate for fuel cell application?
- How a modular converter can improve performance of the fuel cell converter?

In order to achieve these aims the work is performed in several areas. Following main areas are covered in this thesis:

- Modeling – averaged models of various dc-dc step-up converters are developed. Also particular components and parts of dc-dc converters are modeled in relation to power loss and heat dissipation in these components. Combining averaged circuit model and component model will result in robust modeling tool to estimate power losses and efficiency of the converter circuit under specific operational conditions.
- Analysis – different power electronic circuits are analyzed and their features and performance are evaluated on a common basis. Efficiency is one of the most important factors.
- Optimization – selected converters are being designed and optimized according to project limitations.

- Modularization – parallel operation of several modules and its impact on overall system performance is investigated. Special attention is on efficiency improvement by intelligent usage of modules.

1.4.1 Project limitations

The work performed in this thesis is done under following conditions:

- The focus is on dc-dc non-isolated step-up converters only
- The focus is on the converter's power stage only
- Input voltage range is 30 V to 60 V dc
- Output voltage is 400 V dc (for the SVS inverter) or ± 400 V dc (for the half-bridge inverter)
- Power level range is from few hundred watts up to few kilowatts per module
- Converter design incorporates current state of the art components and materials
- Best case efficiency target is 98%
- Input current ripples should be reduced

1.4.2 Used tools

The general purpose simulation program MATLAB/Simulink® is chosen as the main simulation and calculation tool in this project. It supports equation based calculations prepared as script files as well as graphical signal flow simulations prepared as Simulink models.

Power electronic circuit simulations are supported by PLECS® [18] which is a toolbox for MATLAB/Simulink®. It allows control of circuit simulations by simple, often iterative scripts thus many time-consuming simulations are done automatically.

For more advanced design and optimization of magnetic components a simulator called FEMM 4.0.1 [19] is used. This software incorporates finite element methods (FEM) for electromagnetic fields simulations. It's a simple and robust tool providing reliable results within a short time. More advanced users may use FEMM 4.0.1 software in connection with MATLAB® and prepare scripts i.e. for an inductor winding or an air gap optimization.

1.5 Thesis outline

The thesis is divided into seven chapters and an appendix. It begins with broad overview on applications for dc-dc step-up converters and important aspects of non-isolated ones. Various converter topologies are introduced too. Next, different power loss mechanisms present in dc-dc converters are described and reader is guided thru optimization process. Then a modular converter concept is introduced and it's demonstrated how the modular converter can improve a power conversion efficiency.

- Chapter 1 - Introduction
This chapter. Includes background, motivation, application description, problem definition and project limitations. Also it describes general tools used.
- Chapter 2 - Non-Isolated Dc-Dc Converters
An overview on different approaches for boosting of a dc voltage and current state-of-the-art non-isolated step-up dc-dc converters is given. Next, more detailed description and analysis of selected converters is done. Then converters are compared against basic boost converter and against each other. Required passive components, number and utilization of semiconductors, etc. are taken into account. These factors approximate future converter size and cost in compare with other solutions.
- Chapter 3 - Power Losses in Dc-Dc Converters
In this chapter issues related to power losses in dc-dc converters are discussed. First modeling approach is presented. Then sources of major losses are pointed and appropriate models are introduced. These models bases on references, but some of them require minor adjustments. Finally suitable converter models are developed and simulation results are presented. Results shall indicate potential peak efficiency of each topology, thus it's possible to justify them in terms usability in a high voltage gain and high efficiency applications.
- Chapter 4 - Design and Optimization of the Converter
Optimization is a critical part of the converter design process. It results may lead to good or bad design. This chapter describes optimization of the selected converter with special focus on magnetic components.
- Chapter 5 - Modular Converter
Modularity of a power converter is not a new approach. First it was used in telecom, space or military applications. Recently it can be found in commercial products too. It's well known that modular architecture reduces costs of production and maintenance, improves reliability, enables system scalability etc. In this chapter impact on system power conversion efficiency is being investigated. An example application will be fuel cell based UPS, which operates under variable load and variable input voltage, so optimization of a solid converter become difficult.
- Chapter 6 - Experimental results
Report from the converter build-up process and laboratory work is presented in this Chapter. First laboratory equipment and measurement setup is being presented. Next, measured electrical values of magnetic components are provided and compared with calculated values. Finally, efficiency of three breadboards is measured and presented.
- Chapter 7 - Conclusion
This chapter summarize and conclude the whole project, points out findings and suggests future work.

- Appendix A - Publications
Conference papers related to and published during the project period by the author of this thesis are provided to leader in this appendix.
- Appendix B - Models
In this appendix source code of converters and components models used are provided. It also contains C-code of the multiphase PWM generator using microcontroller.

1.6 List of publications

- P. Klimczak and S. Munk-Nielsen, "A single switch dual output non-isolated boost converter," in Applied Power Electronics Conference and Exposition, 2008. APEC 2008. Twenty-Third Annual IEEE, 2008, pp. 43-47.
- P. Klimczak and S. Munk-Nielsen, "Comparative study on paralleled vs. scaled dc-dc converters in high voltage gain applications," in Power Electronics and Motion Control Conference, 2008. EPE-PEMC 2008. 13th, 2008, pp. 108-113.
- P. Klimczak and S. Munk-Nielsen, "Boost Converter with Three-State Switching Cell and Integrated Magnetics," in Applied Power Electronics Conference and Exposition, 2009. APEC 2009. Twenty-Fourth Annual IEEE, 2009, pp. 1378-1383.
- P. Klimczak and S. Munk-Nielsen, "High Efficiency Boost Converter with Three State Switching Cell," in International Exhibition & Conference for Power Electronics, Intelligent Motion, Power Quality PCIM Europe 2009 Nurnberg, Germany, 2009.
- P. Klimczak and S. Munk-Nielsen, "Integration of Magnetic Components in a Step-Up Converter for Fuel Cell," in European Conference on Power Electronics and Applications, 2009. EPE 2009. 13th Barcelona, Spain, 2009.

Chapter 2

Non-Isolated Dc-Dc Converters

There are many different applications for dc-dc boost converters. One of them is a low/medium power fuel cell based UPS systems. In this application boost converter is used to boost the low variable voltage from the fuel cell (or the battery) and provide the high quality, regulated dc voltage to the inverter. For many years isolated topologies with high frequency step-up transformer have been used commonly. However, if there is no need for galvanic isolation between the input and the output of the converter a non-isolated step-up converter might be an interesting and beneficial solution.

Many non-isolated step-up converters were found during a literature study. In following section a general overview on different voltage amplification techniques is given first. Next, several step-up topologies are presented and described in details – starting from the simplest boost converter and ending up with so called non-isolated two-inductor boost converter.

2.1 General overview on non-isolated dc-dc step-up converters

One approach for step-up converter bases on the switched-capacitor principle – charging a number of capacitors in parallel and discharging them in series [20, 21]. However “pure” switched capacitor circuit require significant number of stages to achieve high voltage gain. It means large number of elements (capacitors, diodes and transistors). Moreover control of the output voltage is limited and voltage conversion ratio depends strongly on the circuit configuration. The advantage of this solution is absence of any magnetic devices, so the converter can be very compact – could be even assembled as an integrated circuit (IC). In [22] switched capacitor step-up converter is integrated with boost converter in order to have high voltage gain with reasonable duty ratio and good efficiency. Also boost converter has a regulation purpose, so output voltage is controlled well. Another switched capacitor converter is proposed in [23] – in this paper basic concept bases on resonant energy transfer among the switched capacitors. The converter voltage transfer ratio is determined by the number of stages and fixed.

Another approach is presented in [5, 18, 24-28], where a family of converters with a coupled-inductor (a tapped-inductor, an autotransformer) is introduced. Using coupled inductors these converters can provide a high voltage gain without

extreme duty cycle. However the leakage inductance of the coupled inductor may cause an additional voltage stress on the active switch, so the switching loss increases and the converter's efficiency decreases. Employing a snubber circuit voltage stress (voltage spikes) on the active switch can be attenuated, thus a low voltage rated transistor with a lower on-state resistance can be utilized. In the references [5, 28] a boost converter with a high voltage gain (up to 20) and a very good efficiency (up to 97%) is presented. This converter bases on the coupled-inductor principle, but it incorporates a series capacitor in order to increase the voltage gain. Also, a passive regenerative snubber recovers energy stored in the leakage inductance, ensuring a good performance of this topology. Reference [29] presents a boost converter with a coupled inductor and a voltage multiplier (a voltage doubler). In this converter the output voltage is a sum of the output voltage from the boost converter stage and the voltage multiplier stage.

A similar idea (a boost converter and a voltage multiplier) is presented in [30]. In this paper there is a number of parallel and interleaved strings. Each string contains the boost converter and a number of voltage multiplier stages. However to ensure a high voltage gain at a low duty cycle a number of multiplier stages is required. So, for a higher power and a high voltage gain a large number of parallel and series connected stages is used, so the structure become complex and potentially expensive. Also paralleled strings have a lot of interconnections one to the others, thus reliability of the whole system decreases.

A converter based on a three-state switching cell and a voltage doubler is presented in [31] and it presents a very good efficiency. This converter provides a high voltage gain, a reduced voltage stress on transistors and ensures reduced input current ripples. This converter can be considered as a non-isolated push-pull-boost converter. This topology is presented in details in section 2.2.6.

References [32-34] present a family of Luo converters with a positive and a negative output voltage. Luo converters family comes from SEPIC and ZETA (dual-SEPIC) converters. A voltage gain of the elementary circuit can be increased by using a voltage lift technique and an auxiliary circuit. This auxiliary circuit contains capacitors, diodes and inductors. There are self-lift, re-lift and multiple lift circuits presented in the literature. Self-lift Luo converter in continuous conduction mode (CCM) has the same voltage transfer function like the basic boost converter in CCM, but Luo converter contains significantly more elements and it has a large ripple in the input current. I.e. quadruple-lift Luo converter in CCM has voltage gain 4 times higher than the basic boost converter in CCM, but Luo converter is very complex now and it contains a lot of components (2 active switches, 7 diodes, 6 capacitors and 5 inductors [34]). One can find more about Luo converters and this voltage boost (voltage lift) technique in [35].

All of converter groups presented above are dc-dc converters which regulate voltage in a dc-link. It means that in all cases power conversion has at least two stages. A Z-source inverter is introduced in [36, 37]. It combines a boost converter and an inverter in one stage converter. The reference [36] presents comparison of the Z-source inverter and the boost-buck inverter. In this comparison the boost-buck inverter achieves slightly better efficiency in whole

range of the output power. Number of components is similar in both converters, but the Z-source inverter exerts serious voltage and current stress on the components.

At the moment topology based on a coupled inductor or a three-state switching cell seem to be good candidate for future investigation, because of its high conversion ratio, proved high efficiency, low voltage transistors and overall low component count. However converters with a coupled inductor reveal a common drawback – large ripples in the input current.

2.2 Review of topologies

This section presents several basic non-isolated dc-dc step-up topologies. It includes a converter diagram, main waveforms and short operation description. Key parameters and equations are presented for each topology. Design equations developed in following paragraphs are used at the end of the chapter to compare presented topologies one against the other. Based on the comparison the best candidate topology is selected for future investigation.

Because of requirement of a small input current ripple it is assumed that a converter operates in CCM most of the time. Also it's assumed that all capacitors are large, so capacitor voltages have major dc component with a very small and negligible ripple. Finally, for sake of simplicity it's assumed that all circuits are lossless, thus (2.1) and (2.2) are fulfilled.

$$V_{\text{out}} = M \cdot V_{\text{in}} \quad (2.1)$$

$$I_{\text{in}} = M \cdot I_{\text{out}} \quad (2.2)$$

2.2.1 Basic boost converter

Figure 2.1 presents a boost converter, which is a basic and well-known circuit with voltage step-up capability. In CCM there are only two stages over a single switching period and main waveforms are presented on Figure 2.2. During stage 1 the transistor T_1 is turned-on, the input voltage V_{in} is being applied to the inductor L_1 , the input current $i_{\text{in}}(t)$ increases and the inductor L_1 stores energy. The diode D_1 is reverse biased and the load R_{out} is supplied from the capacitor C_1 . During stage 2 the transistor T_1 is turned-off and the diode D_1 conducts and the inductor L_1 passes stored energy to the output capacitor C_1 . The input current i_{in} decreases.

In CCM the converter's voltage gain M is given by (2.3). The transistor T_1

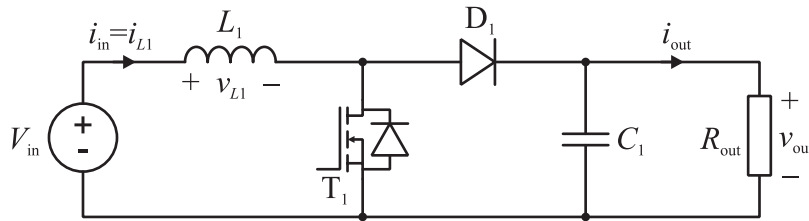


Figure 2.1 Diagram of a basic boost converter

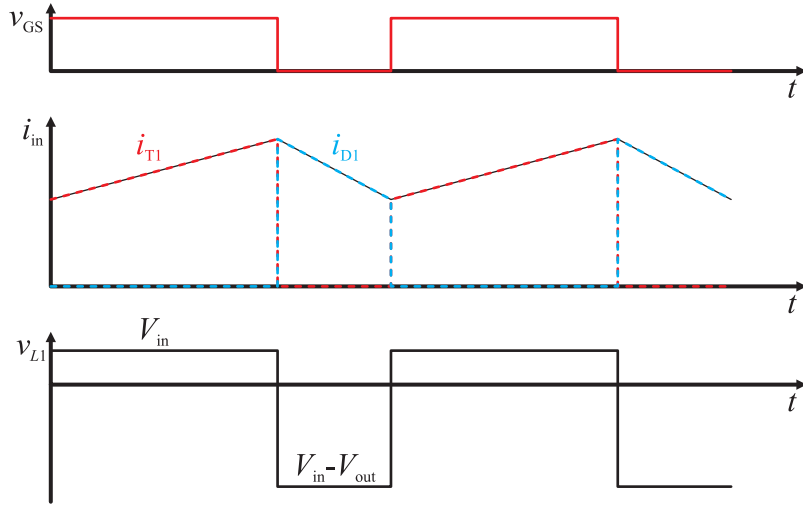


Figure 2.2 Waveforms of a basic boost converter

blocking voltage V_{T1} and diode D_1 reverse voltage V_{D1} are equal to the output voltage V_{out} (under assumption of small output voltage ripple). The transistor rms current $I_{T1(rms)}$ is given by (2.4). The diode average forward current is equal to the average output current. Required power rating of the transistor and the diode in terms of the output power P_{out} are given by (2.5) and (2.6) respectively. For a small input current ripple and a very large duty cycle the rms current is approximated by the dc value. Required inductance L_1 depends on parameters like input voltage V_{in} , switching frequency f_s , duty cycle D and allowed input current ripple Δi_{in} and it's given by (2.7). Output capacitor C_1 size is given by (2.8), where Δv_{out} is allowed amplitude of the output voltage ripple.

$$M = \frac{1}{1-D} \quad (2.3)$$

$$I_{T1(rms)} = I_{in} \cdot \sqrt{1 + \frac{1}{3} \cdot \left(\frac{\Delta i_{in}}{I_{in}} \right)^2} \cdot \sqrt{D} \approx M \cdot I_{out} \quad (2.4)$$

$$\text{volt} \times \text{amp}_{T1} = V_{T1(off)} \cdot I_{T1(rms)} \approx V_{out} \cdot M \cdot I_{out} = M \cdot P_{out} \quad (2.5)$$

$$\text{volt} \times \text{amp}_{D1} = V_{out} \cdot I_{out} \approx P_{out} \quad (2.6)$$

$$L_1 = \frac{V_{in} \cdot D}{2 \cdot \Delta i_{L1} \cdot f_s} \quad (2.7)$$

$$C_1 = \frac{I_{out} \cdot D}{2 \cdot \Delta v_{out} \cdot f_s} \quad (2.8)$$

This topology has an advantage of robustness and simplicity. However fairly large inductor and very poor utilization of the transistor are main drawbacks of this topology operating in a high voltage gain application.

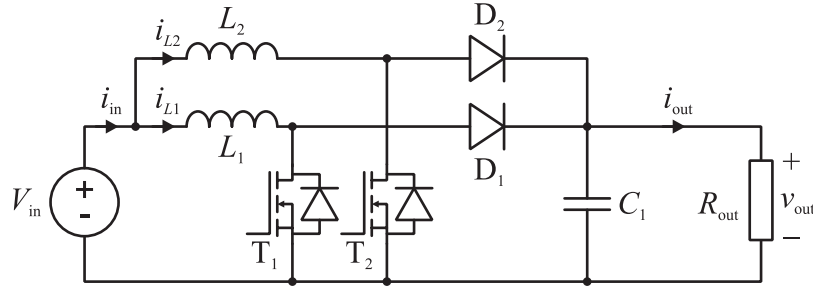


Figure 2.3 Diagram of a 2-phase boost converter

2.2.2 Multi-phase boost converter

Use of several boost converters in parallel expands the output power of the whole system, while the input current is shared between two or more converter modules. Operation with interleaved switching scheme gives an advantage of reduction of the input current ripple and it leads to inductor size reduction. Additionally the output voltage ripple is reduced too, so the output capacitor C_1 can be reduced. Figure 2.3 presents the two phase boost converter. It's composed of two paralleled boost converters which inputs and outputs are connected in parallel. If both converters are identical and transistors are operated with the same duty cycles then the input current is shared equally among paralleled converters.

The multi-phase boost converter operates in the same way like the basic boost converter does. Figure 2.4 presents key waveforms of the two phase boost converter. Gating signals for both transistors have the same duty cycle and they are phase shifted by 180° (interleaving). One may observe that the input current ripple is smaller than ripples observed in particular inductor currents. Main challenge in case of paralleled boost converters is to provide exactly the same duty cycle for all transistors. Even a small mismatch in duty cycles may lead to a significant current sharing unbalance and reduce reliability of the system. Different active and passive current sharing methods are discussed in [38].

In case of paralleled converters the voltage gain M does not change and it's given by (2.9). Also transistors' blocking voltage and diodes' reverse voltage doesn't change and are about the output voltage V_{out} . The transistor rms current is given by (2.10). A significant inductor current ripple cannot be neglected this time and it has an influence on the transistor power rating according to (2.11). Term N means number of paralleled modules, sharing the input current. Required power rating of the diode D_1 is given by (2.12). The required inductance L_1 is given by (2.13).

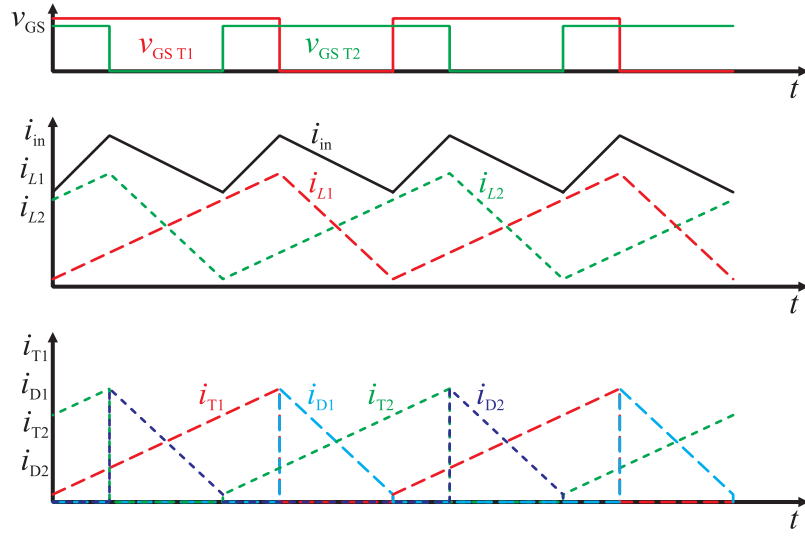


Figure 2.4 Waveforms of a 2-phase boost

It's important to note that allowed inductor current ripple may become significantly larger than allowed input current ripple ($\Delta i_{L1} > \Delta i_{in}$), thus required inductance L_1 can be reduced. The current ripple reduction for depends on number of interleaved phases and duty cycle. Simulation results for 2, 4, and 8 phase interleaved boost converter are presented on Figure 2.5. However one should be aware that increased inductor current ripple may lead to increased ac copper losses in the inductor winding and increased conduction losses in the transistor.

$$M = \frac{1}{1-D} \quad (2.9)$$

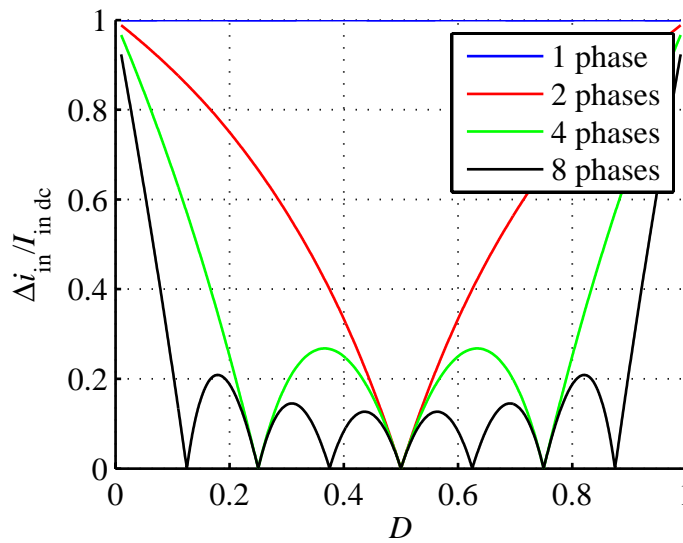


Figure 2.5 Reduction of the relative input current ripple in a multi phase boost converter

$$I_{T1(\text{rms})} = \frac{I_{\text{in}}}{N} \cdot \sqrt{1 + \frac{1}{3} \cdot \left(\frac{\Delta i_{L1}}{I_{L1}} \right)^2} \cdot \sqrt{D} \approx \frac{M}{N} \cdot I_{\text{in}} \cdot \sqrt{1 + \frac{1}{3} \cdot \left(\frac{\Delta i_{L1}}{I_{L1}} \right)^2} \quad (2.10)$$

$$\begin{aligned} \text{volt} \times \text{amp}_{T1} &= V_{T1(\text{off})} \cdot I_{T1(\text{rms})} \approx V_{\text{out}} \cdot \frac{M}{N} \cdot I_{\text{in}} \cdot \sqrt{1 + \frac{1}{3} \cdot \left(\frac{\Delta i_{L1}}{I_{L1}} \right)^2} = \\ &= \frac{M}{N} \cdot P_{\text{out}} \cdot \sqrt{1 + \frac{1}{3} \cdot \left(\frac{\Delta i_{L1}}{I_{L1}} \right)^2} \end{aligned} \quad (2.11)$$

$$\text{volt} \times \text{amp}_{D1} = V_{\text{out}} \cdot \frac{I_{\text{out}}}{N} \approx \frac{P_{\text{out}}}{N} \quad (2.12)$$

$$L_1 = \frac{V_{\text{in}} \cdot D}{2 \cdot \Delta i_{L1} \cdot f_s} \quad (2.13)$$

$$C_1 = \frac{I_{\text{out}} \cdot D}{2 \cdot \Delta v_{\text{out}} \cdot f_s \cdot N} \quad (2.14)$$

Furthermore two inductors, L_1 and L_2 , can be coupled together on a single magnetic core resulting in a two phase boost converter with a coupled inductor, like the one presented on Figure 2.6. The coupled inductor is presented as an ideal transformer with two identical windings $n_1=n_2$, and a storage inductance L_M in parallel to the winding n_1 . Key waveforms of this converter are presented on Figure 2.7. It is important to note that this converter operates with the transistor duty cycle below 50%, i.e. without overlapping. In CCM there are four basic operation stages over a single transistor switching period. During stage 1 both transistors are turned-off and energy stored in the inductance L_M is being released thru diodes D_1 and D_2 to the output capacitor C_1 . The input current splits into two identical halves and flows thru both windings n_1 and n_2 . At the beginning of stage 2 the transistor T_1 is turned-on. Input voltage V_{in} is applied to the winding n_1 . The same voltage induces in the winding n_2 , but it's too low to forward bias the body diode of the transistor T_2 , so there is no current flow in the winding n_2 . During this stage the whole input current $i_{\text{in}}(t)$ flows thru the winding n_1 . Energy is stored in the storage inductance L_M . Stage 3 is identical to the stage 1 while both transistors are turned-off. Stage 4 is symmetrical to the stage 2, but the transistors T_2 is being turned-on and T_1 remains turned-off.

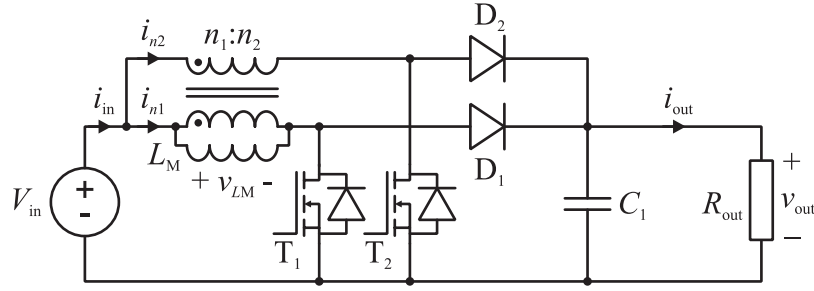


Figure 2.6 Diagram of a two phase boost converter with a coupled inductor

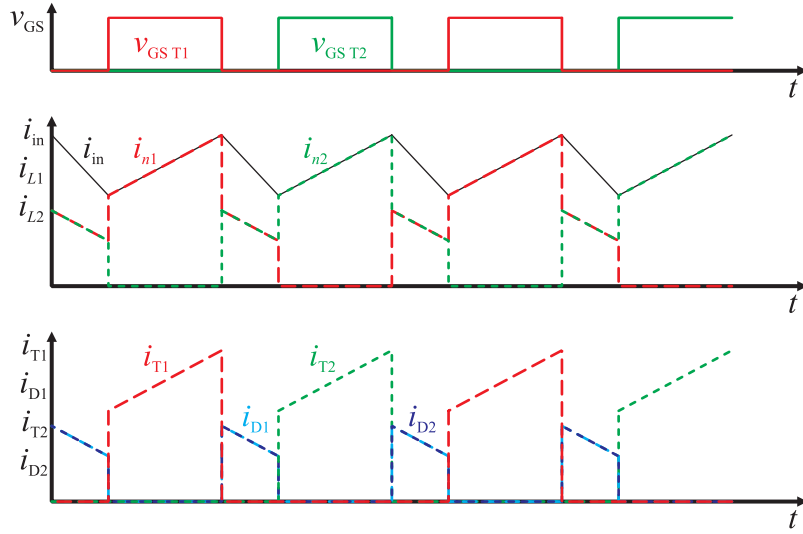


Figure 2.7 Waveforms of a 2-phase boost converter with a coupled inductor

In CCM the voltage gain M is given by (2.15). The transistors' blocking voltage and diodes' reverse voltage doesn't change and are about the output voltage V_{out} . The transistor rms current is given by (2.16) and the transistor power rating is given by (2.17). Both diodes share the output current equally and the diode power rating is given by (2.18). The effective frequency "seen" by the coupled inductor L_M and the output capacitor C_1 is double of the switching frequency f_s . It enables use of a smaller inductor (2.19) and a smaller capacitor (2.20), in compare to the basic boost converter.

$$M = \frac{1}{1-2 \cdot D} \quad (2.15)$$

$$I_{T1(rms)} = I_{in} \cdot \sqrt{1 + \frac{1}{3} \cdot \left(\frac{\Delta i_{in}}{I_{in}} \right)^2} \cdot \sqrt{D} \approx M \cdot \sqrt{D} \cdot I_{out} \quad (2.16)$$

$$\text{volt} \times \text{amp}_{T1} = V_{T1(off)} \cdot I_{T1(rms)} \approx V_{out} \cdot M \cdot \sqrt{D} \cdot I_{out} = M \cdot \sqrt{D} \cdot P_{out} \quad (2.17)$$

$$\text{volt} \times \text{amp}_{D1} = V_{out} \cdot \frac{I_{out}}{2} \approx \frac{P_{out}}{2} \quad (2.18)$$

$$L_1 = \frac{V_{in} \cdot D}{2 \cdot \Delta i_{LM} \cdot f_s} \quad (2.19)$$

$$C_1 = \frac{I_{out} \cdot D}{2 \cdot \Delta v_{out} \cdot f_s} \quad (2.20)$$

The boost converter with the coupled inductor overcomes current sharing problem [39] and with proper winding arrangement results in compact and efficient design of the coupled inductor, even in spite of significant ac component in winding currents [40].

2.2.3 Cascaded boost converter

Theoretically a basic boost converter is able to provide infinite voltage gain while duty cycle approaches 100% according to (2.3). However the basic boost converter has the voltage gain from 2-5 in products [41] up to 15-20 in breadboards [42].

The limitation of the voltage gain comes from two major directions. On the one hand parasitics present in the power circuit should be taken into account, while resistive losses in the inductor, in the transistor and in the diode effectively limit the maximum voltage gain [43]. Also the converter with a very large voltage gain requires oversized transistor according to (2.5). Such high voltage transistor usually exhibits a high on-state resistance. In connection with a large input current results in a high conduction loss, which limits both, efficiency and rated power of the converter module. On the other hand the voltage gain curve become steeper while duty cycle increases. At one point it's fairly difficult to control the converter, while a very small variation in duty cycle D results in a large change in the voltage gain M . This small variation in the duty cycle D may be desired, as a response to change of operating conditions. But it can be undesired, e.g. caused by delays in the driver circuit or different switching of the transistor due to the temperature or ageing.

If a very high voltage gain is required it may be more beneficial to use of two or more series connected (cascaded) boost converters, like presented on Figure 2.8. This approach gives some advantages, but it creates new challenges in the same time. Main advantages include a high voltage gain, a good power decoupling between the output and the input, better utilization of semiconductors, presence of an intermediate dc bus. Major drawbacks are more complex circuit, more complex controls and a potential stability problem.

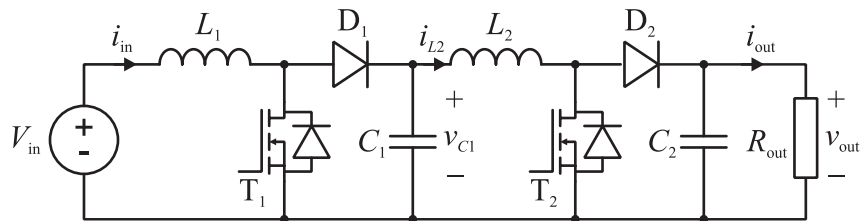


Figure 2.8 Diagram of a cascaded boost converter

The voltage gain of the cascaded boost converter operating in CCM is the product of the voltage gain of each stage (2.21). The transistor T_1 and the diode D_1 have to handle the intermediate voltage V_{C1} , while the transistor T_2 and the diode D_2 have to handle the output voltage V_{out} . Transistors' rms currents are given by (2.22) and (2.23), under assumption of a small input current ripple and a large intermediate current ripple. Required power rating of both transistors is the sum of respective power ratings and it's given by (2.26). Similarly the requires power rating of both diodes is given by (2.29). For a large voltage gain M cascading of two or more boost converters lead to a significant reduction of the required transistors power rating, but in the same time it increases required diodes power rating by number of cascaded converter stages.

It's important to note that "smooth" input current is ensured by the inductor L_1 only (2.30). The capacitor C_2 determines the output voltage ripple (2.33). The intermediate voltage $v_{C1}(t)$ and the intermediate current $i_{L2}(t)$ may contain larger ripples, so the capacitor C_1 and the inductor L_2 can be reduced – equations (2.32) and (2.31) respectively. Moreover the transistor T_1 can operate with higher switching frequency then the transistor T_2 can, i.e. $f_{s1} > f_{s2}$. It allows to reduce the inductance L_1 and capacitance C_1 further.

$$M = M_1 \cdot M_2 = \frac{1}{1-D_1} \cdot \frac{1}{1-D_2} \quad (2.21)$$

$$I_{T1(rms)} = I_{in} \cdot \sqrt{1 + \frac{1}{3} \cdot \left(\frac{\Delta i_{in}}{I_{in}} \right)^2} \cdot \sqrt{D_1} \approx M_1 \cdot M_2 \cdot \sqrt{D_1} \cdot I_{out} \quad (2.22)$$

$$I_{T2(rms)} = I_{L2} \cdot \sqrt{1 + \frac{1}{3} \cdot \left(\frac{\Delta i_{L2}}{I_{L2}} \right)^2} \cdot \sqrt{D_2} \approx \quad (2.23)$$

$$\approx M_2 \cdot \sqrt{D_2} \cdot \sqrt{1 + \frac{1}{3} \cdot \left(\frac{\Delta i_{L2}}{I_{L2}} \right)^2} \cdot I_{out}$$

$$\text{volt} \times \text{amp}_{T1} = V_{T1(off)} \cdot I_{T1(rms)} \approx \frac{V_{out}}{M_2} \cdot M_1 \cdot M_2 \cdot \sqrt{D_1} \cdot I_{out} = M_1 \cdot \sqrt{D_1} \cdot P_{out} \quad (2.24)$$

$$\text{volt} \times \text{amp}_{T2} = V_{T2(off)} \cdot I_{T2(rms)} \approx V_{out} \cdot M_2 \cdot \sqrt{D_2} \cdot \sqrt{1 + \frac{1}{3} \cdot \left(\frac{\Delta i_{L2}}{I_{L2}} \right)^2} \cdot I_{out} = \quad (2.25)$$

$$= M_2 \cdot \sqrt{D_2} \cdot \sqrt{1 + \frac{1}{3} \cdot \left(\frac{\Delta i_{L2}}{I_{L2}} \right)^2} \cdot P_{out}$$

$$\begin{aligned} \text{volt} \times \text{amp}_T &= \text{volt} \times \text{amp}_{T1} + \text{volt} \times \text{amp}_{T2} = \\ &= \left(M_1 \cdot \sqrt{D_1} + M_2 \cdot \sqrt{D_2} \cdot \sqrt{1 + \frac{1}{3} \cdot \left(\frac{\Delta i_{L2}}{I_{L2}} \right)^2} \right) \cdot P_{out} \end{aligned} \quad (2.26)$$

$$\text{volt} \times \text{amp}_{D1} = \frac{V_{\text{out}}}{M_2} \cdot I_{\text{out}} \cdot M_2 \approx P_{\text{out}} \quad (2.27)$$

$$\text{volt} \times \text{amp}_{D2} = V_{\text{out}} \cdot I_{\text{out}} \approx P_{\text{out}} \quad (2.28)$$

$$\text{volt} \times \text{amp}_D = \text{volt} \times \text{amp}_{D1} + \text{volt} \times \text{amp}_{D2} = 2 \cdot P_{\text{out}} \quad (2.29)$$

$$L_1 = \frac{V_{\text{in}} \cdot D_1}{2 \cdot \Delta i_{\text{in}} \cdot f_{s1}} \quad (2.30)$$

$$L_2 = \frac{V_{C1} \cdot D_2}{2 \cdot \Delta i_{L2} \cdot f_{s2}} \quad (2.31)$$

$$C_1 = \frac{I_{L2} \cdot D_1}{2 \cdot \Delta v_{C1} \cdot f_{s1}} \quad (2.32)$$

$$C_2 = \frac{I_{\text{out}} \cdot D_2}{2 \cdot \Delta v_{\text{out}} \cdot f_{s2}} \quad (2.33)$$

In order to extend power level of the cascaded boost converter it's possible to parallel one or more cascaded stages.

2.2.4 Center tapped boost converter

A basic configuration of a center-tapped boost converter [25, 27] is presented on Figure 2.9. The converter is similar to the two stage cascaded boost converter (Figure 2.8) but there is no second transistor T_2 . Instead, two inductors L_1 and L_2 are magnetically coupled now and they form the coupled inductor, also called an autotransformer or a center tapped inductor. In fact this coupled inductor works in the way similar to a flyback transformer. The coupled inductor is modeled as a two winding ideal transformer $n_1:n_2$ and a storage inductance L_M connected in parallel with the primary winding of the transformer. For sake of simplicity the leakage inductance is neglected. The converter operates in CCM if the magnetizing current $i_{LM}(t)$ (representation of the magnetic flux) is continuous. For simplified analysis it's assumed that there are only two major operating stages in CCM.

The converter main waveforms are presented on Figure 2.10. At the beginning of stage 1 the transistor T_1 is turned on and the input voltage V_{in} is being applied across the winding n_1 and the inductor L_M . Rising input current flows thru storing inductance L_M and the transistor T_1 only. Positive voltage $v_{n2}(t)$ induces in the winding n_2 , the diode D_2 is reverse biased, so there is no current flow in the winding

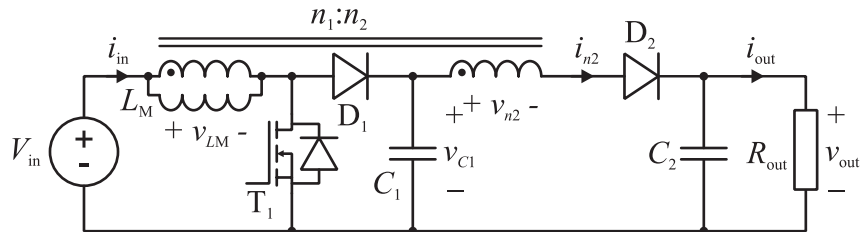


Figure 2.9 Diagram of a center-tapped boost converter

n_2 . Depends on operating point and the turns ratio n is may happen that induced during this stage voltage $v_{n2}(t)$ is larger than the voltage $v_{C1}(t)$. In such case the diode D_2 experience the reverse voltage even larger than the output voltage V_{out} (2.35). During stage 2 the transistor T_1 is turned-off and energy stored in the storage inductance L_M is being released. Voltages across both windings n_1 and n_2 are negative now, so diodes D_1 and D_2 may become forward biased. In an ideal case diode currents are almost identical and their average value is the same. However an exact shape of these currents depend on several factors like: capacitances, diodes forward voltage, winding resistance and leakage inductance, etc.

The voltage gain of the converter is given by (2.36). Required transistor and diode D_1 voltage rating is reduced by the coupled inductor turns ratio n and it's given by (2.37). In the same time the diode D_2 has to handle larger voltage which is given by (2.38). In order to find transistor rms current, first the magnetizing dc current I_{LM} is found with (2.39). Assuming that the magnetizing current has a small ripple then the transistor rms current is found with (2.40). Both diodes conduct the same average current which is equal to the output dc current I_{out} . Power rating of the transistor is given by (2.41) and the power rating of diodes is given by (2.44). Required storage inductance L_M is given by (2.45). The output voltage ripple is limited by the capacitor C_2 which capacitance is given by (2.46). The capacitor C_1 acts as a regenerative snubber. Its capacitance should be large enough to store energy coming from the leakage inductance of the coupled inductor and clamp the voltage $v_{C1}(t)$ at the certain level.

$$n = \frac{n_2}{n_1} \quad (2.34)$$

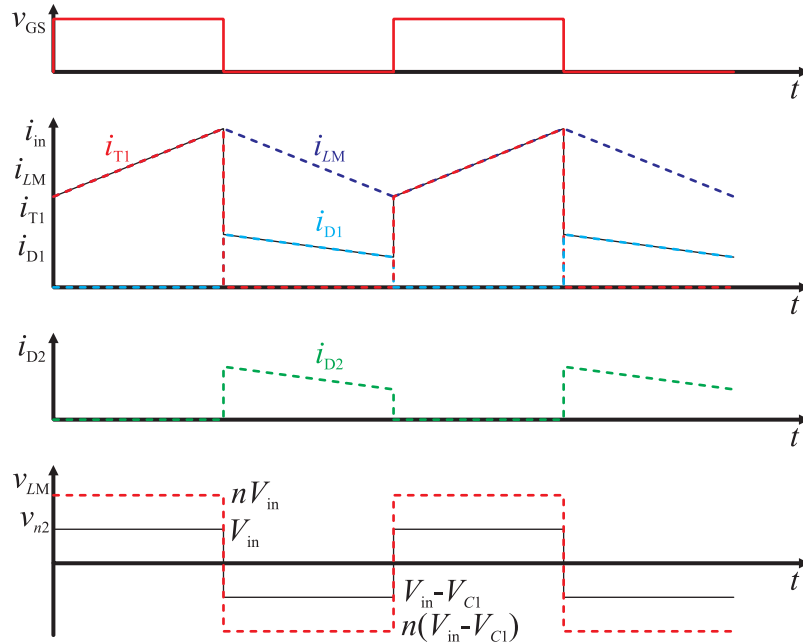


Figure 2.10 Waveforms of the center tapped boost converter

$$v_{C1} < v_{n2} \longrightarrow \frac{1}{1-D} < n \quad (2.35)$$

$$M = \frac{1+n \cdot D}{1-D} \quad (2.36)$$

$$V_{T1(\text{off})} = V_{D1(R)} = \frac{1}{n \cdot D + 1} \cdot V_{\text{out}} \quad (2.37)$$

$$V_{D2(R)} = \frac{n}{n \cdot D + 1} \cdot V_{\text{out}} \quad (2.38)$$

$$I_{LM} = I_{\text{in}} \cdot \frac{n+1}{n \cdot D + 1} = I_{\text{out}} \cdot \frac{\cancel{n \cdot D + 1}}{1-D} \cdot \frac{n+1}{\cancel{n \cdot D + 1}} \quad (2.39)$$

$$I_{T1(\text{rms})} = I_{LM} \cdot \sqrt{D} \cdot \sqrt{1 + \frac{1}{3} \cdot \left(\frac{\Delta i_{LM}}{I_{LM}} \right)^2} \approx \frac{n+1}{1-D} \cdot \sqrt{D} \cdot I_{\text{out}} \quad (2.40)$$

$$\begin{aligned} \text{volt} \times \text{amp}_{T1} &= V_{T1(\text{off})} \cdot I_{T1(\text{rms})} \approx \\ &\approx \frac{1}{n \cdot D + 1} \cdot V_{\text{out}} \cdot \frac{n+1}{1-D} \cdot \sqrt{D} \cdot I_{\text{out}} = M \cdot \frac{n+1}{(n \cdot D + 1)^2} \cdot \sqrt{D} \cdot P_{\text{out}} \end{aligned} \quad (2.41)$$

$$\text{volt} \times \text{amp}_{D1} = \frac{1}{n \cdot D + 1} \cdot V_{\text{out}} \cdot I_{\text{out}} = \frac{1}{n \cdot D + 1} \cdot P_{\text{out}} \quad (2.42)$$

$$\text{volt} \times \text{amp}_{D2} = \frac{n}{n \cdot D + 1} \cdot V_{\text{out}} \cdot I_{\text{out}} = \frac{n}{n \cdot D + 1} \cdot P_{\text{out}} \quad (2.43)$$

$$\text{volt} \times \text{amp}_D = \text{volt} \times \text{amp}_{D1} + \text{volt} \times \text{amp}_{D2} = \frac{1+n}{n \cdot D + 1} \cdot P_{\text{out}} \quad (2.44)$$

$$L_M = \frac{V_{\text{in}} \cdot D}{2 \cdot \Delta i_{LM} \cdot f_s} \quad (2.45)$$

$$C_2 = \frac{I_{\text{out}} \cdot D}{2 \cdot \Delta v_{\text{out}} \cdot f_s} \quad (2.46)$$

Major advantages of this topology are a high voltage gain under reasonable duty cycle and reduced voltage stress on the transistor. Unfortunately this topology has several drawbacks. The main one is a large input current ripple determined by turns ratio n . Also the diode D_2 may exhibit increased voltage stress if (2.35) is fulfilled. Finally, the winding arrangement of the coupled inductor may become difficult. First, the storage inductance L_M has to be fairly large, which in connection with a dc bias result in a significant number of turns in the winding n_1 . The winding n_2 has n times more turns. Both windings have to have a low dc and ac resistance in the same time, which is a challenge for a significant number of turns.

More detailed analysis of the converter, including presence of the leakage inductance is presented in [25, 27]. Moreover similar solutions based on a coupled inductors are presented in [5, 18, 24, 26, 28].

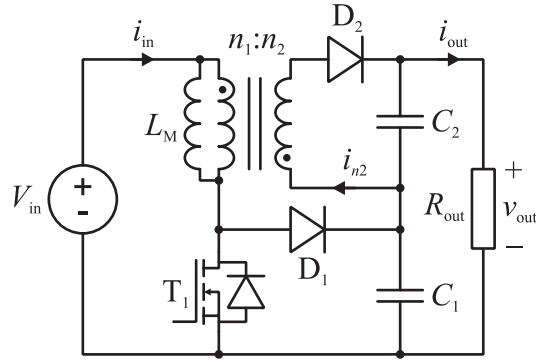


Figure 2.12 Diagram of a flyback-boost converter

2.2.5 Non-isolated flyback-boost converter

A very interesting modification of a flyback converter is presented on Figure 2.12 [19]. In comparison to the original flyback converter this one has two extra components – the diode D_1 and the capacitor C_1 . These additional components act as a regenerative snubber for the transistor T_1 . It overcomes a problem related to a leakage inductance of a flyback transformer. Series connection of capacitors C_1 and C_2 improves the voltage gain M in compare to the original flyback converter too. A flyback transformer $n_1:n_2$ is modeled as an ideal transformer with a storage inductance L_M connected in parallel to the winding n_1 . For sake of simplicity the leakage inductance is neglected. The converter operates in CCM if the magnetizing current $i_{LM}(t)$ (representation of the magnetic flux) is continuous. This simplified analysis includes only two major operating stages in CCM.

Key waveforms of the converter are presented on Figure 2.11. At the beginning

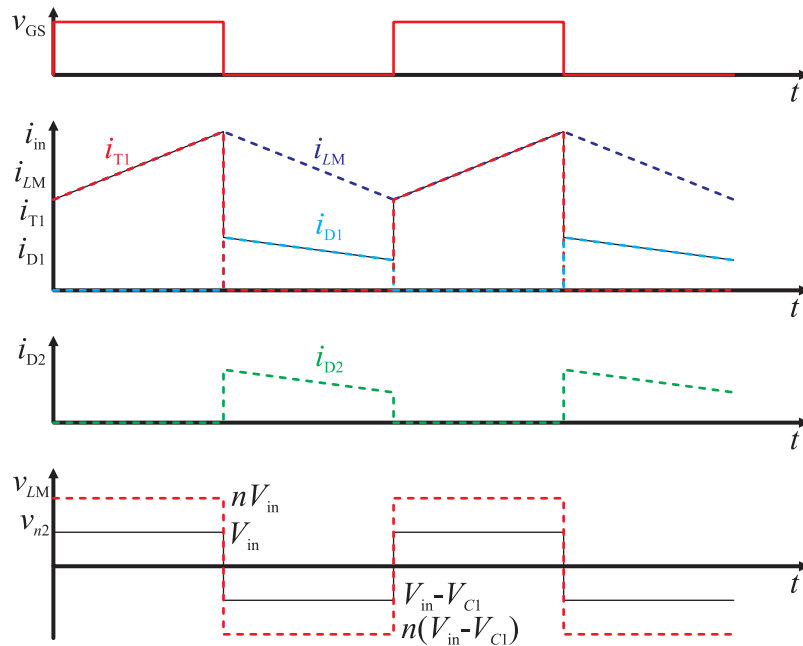


Figure 2.11 Main waveforms of the flyback-boost converter

of stage 1 the transistor T_1 is turned on. The input voltage V_{in} is applied to the winding n_1 and the storage inductor L_M . The diode D_1 is reverse biased and the input current flows thru the storage inductor L_M and the transistor T_1 . Also a positive voltage v_{n2} induced in the winding n_2 and the diode D_2 is reverse biased, so the current i_{n2} is zero during this stage. The load R_{out} is being supplied from output capacitors C_1 and C_2 which are connected in series. During stage 2 the transistor T_1 is off. Energy stored in the inductance L_M is passed thru diodes to capacitors. Both diodes conduct the same average current, but exact shape of each diode current depends on several factors like: output capacitance, diode forward voltage, winding resistance, leakage inductance and so on. In an ideal case both diode currents are almost identical.

The voltage gain of the converter is given by (2.47). The transistor T_1 and the diode D_1 blocking voltages are given by (2.48). The diode D_2 blocking voltage is given by (2.49) and this voltage may exceed the output voltage V_{out} in many cases. The transistor T_1 rms current is found with (2.51), where I_{LM} is the magnetizing dc current given by (2.50). Both diodes conduct the same average current equal to the output dc current I_{out} . With these information required power ratings of all semiconductors are found with equations (2.52) to (2.55). The converter requires fairly large output capacitors since they are connected in series and the effective output capacitance is given by (2.57). Finally (2.56) gives required value of the storage inductance L_M .

$$M = \frac{1 + n \cdot D}{1 - D} \quad (2.47)$$

$$V_{T1(off)} = V_{D1(R)} = \frac{1}{1 + n \cdot D} \cdot V_{out} \quad (2.48)$$

$$V_{D2(R)} = \frac{n}{1 + n \cdot D} \cdot V_{out} \quad (2.49)$$

$$I_{LM} = I_{out} \cdot \frac{n + 1}{1 - D} \quad (2.50)$$

$$I_{T1(rms)} = I_{LM} \cdot \sqrt{D} \cdot \sqrt{1 + \frac{1}{3} \cdot \left(\frac{\Delta i_{LM}}{I_{LM}} \right)^2} \approx \frac{n + 1}{1 - D} \cdot \sqrt{D} \cdot I_{out} \quad (2.51)$$

$$\begin{aligned} \text{volt} \times \text{amp}_{T1} &= V_{T1(off)} \cdot I_{T1(rms)} \approx \\ &\approx \frac{1}{n \cdot D + 1} \cdot V_{out} \cdot \frac{n + 1}{1 - D} \cdot \sqrt{D} \cdot I_{out} = M \cdot \frac{n + 1}{(n \cdot D + 1)^2} \cdot \sqrt{D} \cdot P_{out} \end{aligned} \quad (2.52)$$

$$\text{volt} \times \text{amp}_{D1} = \frac{1}{n \cdot D + 1} \cdot V_{out} \cdot I_{out} = \frac{1}{n \cdot D + 1} \cdot P_{out} \quad (2.53)$$

$$\text{volt} \times \text{amp}_{D2} = \frac{n}{n \cdot D + 1} \cdot V_{out} \cdot I_{out} = \frac{n}{n \cdot D + 1} \cdot P_{out} \quad (2.54)$$

$$\text{volt} \times \text{amp}_D = \text{volt} \times \text{amp}_{D1} + \text{volt} \times \text{amp}_{D2} = \frac{1+n}{n \cdot D+1} \cdot P_{\text{out}} \quad (2.55)$$

$$L_M = \frac{V_{\text{in}} \cdot D}{2 \cdot \Delta i_{LM} \cdot f_s} \quad (2.56)$$

$$C_{\text{out}} = \frac{I_{\text{out}} \cdot D}{2 \cdot \Delta v_{\text{out}} \cdot f_s} \quad (2.57)$$

This converter has the same voltage gain like the center tapped boost converter presented in section 2.2.4. Also the flyback-boost converter has the same voltage stress on the diode D_2 but it requires larger output capacitors than the center-tapped boost. The flyback-boost converter gives an idea how to transform some of isolated topologies into non-isolated ones by adding the regenerative snubber composed of the diode D_1 and the capacitor C_1 . This approach overcomes problems related to a leakage inductance of a transformer and improves voltage gain in the same time.

2.2.6 Non-isolated push-pull-boost converter

A non-isolated push-pull-boost converter is presented on Figure 2.13. This converter can be derived from a current-fed push-pull [43] converter using the same approach like described in section 2.2.5. Additional components - diodes D_1 , D_{11} and the capacitor C_1 - act as a regenerative snubber, recycling energy stored in a leakage inductance of the push-pull transformer. Also series connection of all capacitors improves the voltage gain M . In literature this topology is also called a boost converter with a three state switching cell and a voltage multiplier [6, 31, 44].

Key waveforms of the converter are presented on Figure 2.14. Basically the converter operates in CCM and with duty cycle above 50% (overlapping mode). Under such conditions there are four major operating stages. Stages 1 and 3 are identical. Both transistors are turned-on and share the input current equally, since both primary windings are effectively connected anti-parallel and $n_1=n_{11}$. During this period the input inductor L_1 is being charged. No voltage induces in the

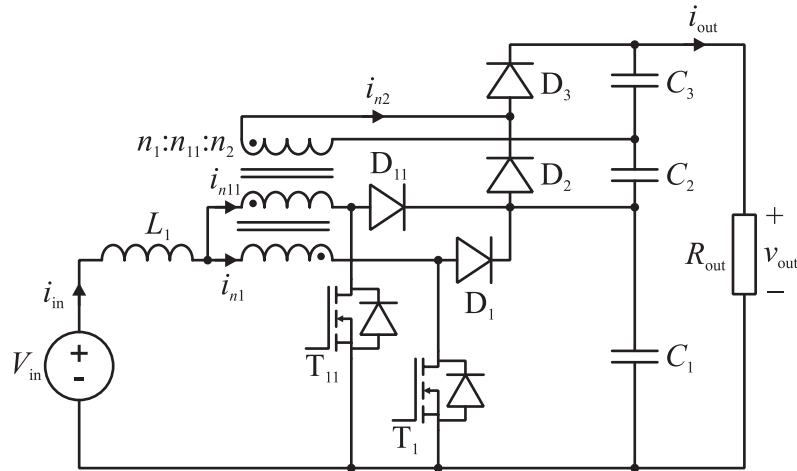


Figure 2.13 Diagram of a non-isolated push-pull-boost converter [6, 31, 44]

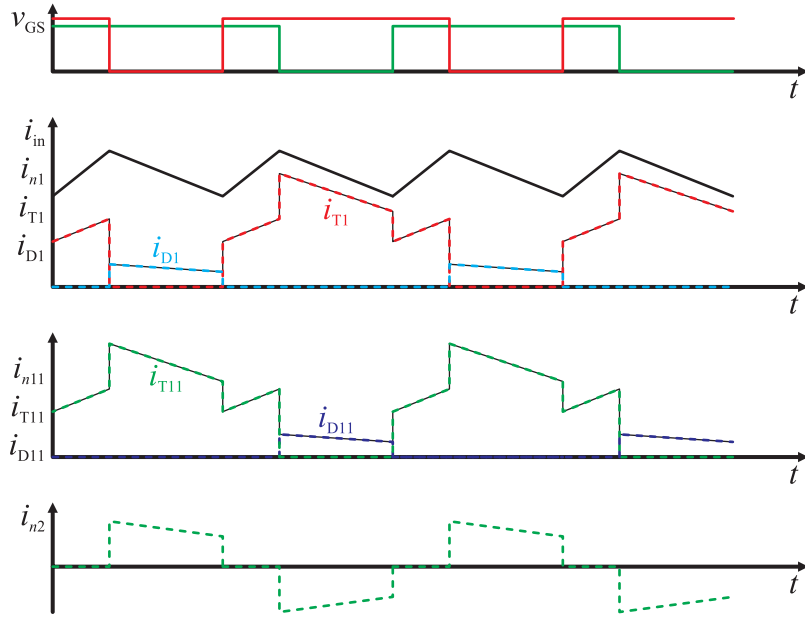


Figure 2.14 Main waveforms of the non-isolated push-pull-boost converter

winding n_2 and there is no current flow in this winding too. Next, at the beginning of stage 2 the transistor T_1 is turned-off. The current i_{n1} continues to flow through the diode D_1 to the capacitor C_1 . During this stage windings n_1 and n_{11} are effectively connected in series and the voltage $v_{C1}(t)$ is applied to them. Positive voltage $v_{n2}(t)$ induces in the winding n_2 , the diode D_3 is forward biased and the capacitor C_3 is recharged during this stage. The last stage 4 is similar to stage 2, but this time the transistor T_1 remains on and the transistor T_{11} is turned-off. During this stage diodes D_{11} and D_2 conduct and capacitors C_1 and C_2 are recharged.

The voltage gain of this converter is given by (2.59). Voltage stress of transistors and diodes D_1 and D_{11} is reduced and given by (2.60). Diodes D_2 and D_3 have to handle reverse voltage given by (2.61). Assuming that the input current had a very small ripple and the current $i_{n2}(t)$ is almost rectangular, the transistor rms current is given by (2.62). The average forward current of diodes D_2 and D_3 is equal to the output dc current I_{out} . The average forward current of diodes D_1 and D_{11} equals half of the output dc current, since these diodes are connected in parallel. Required power rating of transistors and diodes is given by equations (2.63) to (2.67). Required storage inductance L_1 is found with (2.68), while (2.69) gives the effective output capacitance.

$$n = \frac{n_2}{n_1} = \frac{n_2}{n_{11}} \quad (2.58)$$

$$M = \frac{1+n}{1-D} \quad (2.59)$$

$$V_{T1(off)} = V_{T11(off)} = V_{D1(R)} = V_{D11(R)} = \frac{1}{1+n} \cdot V_{out} \quad (2.60)$$

$$V_{D2(R)} = V_{D3(R)} = \frac{n}{n+1} \cdot V_{out} \quad (2.61)$$

$$I_{T1(rms)} \approx \sqrt{(1-D) \cdot \left(\frac{M \cdot I_{out}}{2} + \frac{n}{2} \cdot \frac{I_{out}}{1-D} \right)^2 + (2 \cdot D - 1) \cdot \left(\frac{M \cdot I_{out}}{2} \right)^2} \quad (2.62)$$

$$\begin{aligned} \text{volt} \times \text{amp}_{T1} &= V_{T1(off)} \cdot I_{T1(rms)} \approx \\ &\approx \frac{1}{n+1} \cdot \sqrt{(1-D) \cdot \left(\frac{M}{2} + \frac{n}{2 \cdot (1-D)} \right)^2 + (2 \cdot D - 1) \cdot \left(\frac{M}{2} \right)^2} \cdot P_{out} \end{aligned} \quad (2.63)$$

$$\text{volt} \times \text{amp}_T = 2 \cdot \text{volt} \times \text{amp}_{T1} \quad (2.64)$$

$$\text{volt} \times \text{amp}_{D1} = \frac{1}{n+1} \cdot V_{out} \cdot \frac{I_{out}}{2} = \frac{1}{2 \cdot (n+1)} \cdot P_{out} \quad (2.65)$$

$$\text{volt} \times \text{amp}_{D2} = \frac{n}{n+1} \cdot V_{out} \cdot I_{out} = \frac{n}{n+1} \cdot P_{out} \quad (2.66)$$

$$\text{volt} \times \text{amp}_D = 2 \cdot (\text{volt} \times \text{amp}_{D1} + \text{volt} \times \text{amp}_{D2}) = \frac{1+2 \cdot n}{1+n} \cdot P_{out} \quad (2.67)$$

$$L_1 = \frac{V_{in} \cdot (D - 0.5)}{2 \cdot \Delta i_{in} \cdot f_s} \quad (2.68)$$

$$C_{out} = \frac{I_{out} \cdot D}{2 \cdot \Delta v_{out} \cdot f_s} \quad (2.69)$$

Major advantages of this topology are: high voltage gain, limited input current ripple and reduced voltage stress on transistors. In the same time the converter reveals important drawbacks including: complicated design of the three-winding transformer, three series connected output capacitors and number of diodes effectively connected in series. However even in spite of these drawbacks this topology seems to be a good candidate for a step-up converter for a fuel cell.

2.2.7 Non-isolated two-inductor-boost converter

A non-isolated two-inductor boost converter is presented on Figure 2.15. This converter is derived from a two-inductor boost converter using approach presented in section 2.2.5. Diodes D_1 , D_{11} and the capacitor C_1 act as a regenerative snubber for transistors T_1 and T_{11} .

Key waveforms are presented on Figure 2.16. Basically the converter operates in CCM with duty cycle above 50%. There are four basic operational stages. Stages 1 and 3 are identical. Both transistors are on, the input current $i_{in}(t)$ increases and energy is stored in inductors L_1 and L_2 . The winding n_1 is essentially shorted and no voltage induces in the winding n_2 . All diodes are reverse biased, so the load is supplied from output capacitors. At the beginning of stage 2 the transistor T_1 is turned-off and the diode D_1 starts to conduct because of continuous inductor current $i_{L1}(t)$. The capacitor voltage $v_{C1}(t)$ is being applied to the winding

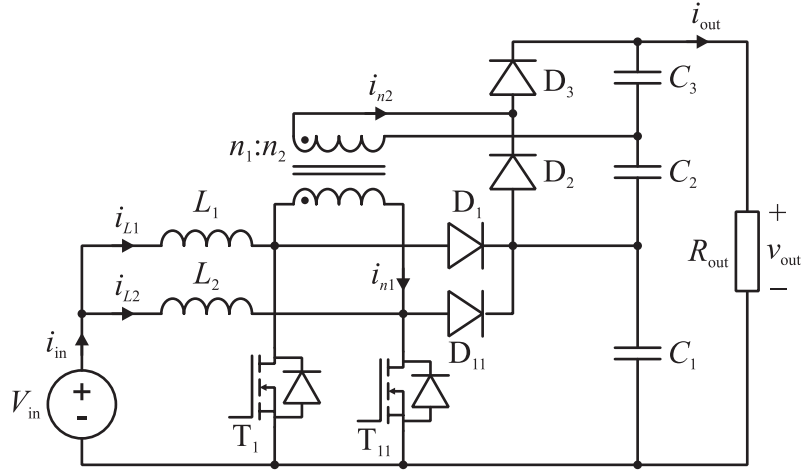


Figure 2.15 Diagram of a non-isolated two-inductor-boost converter

n_1 and voltage $n \cdot v_{C1}(t)$ induces in the winding n_2 . If this voltage is larger than the capacitor voltage $v_{C3}(t)$ then the diode D_3 become forward biased and conducts the current $i_{n2}(t)$ recharging the capacitor C_3 . Stage 4 is similar to stage 2 but the transistor T_{11} is turned-off and T_1 remains on. Diodes D_{11} and D_2 conduct and capacitors C_1 and C_2 are recharged during stage 4.

The voltage gain of this converter is given by (2.71). Voltage stress of transistors and diodes D_1 and D_{11} is given by (2.72). Diodes D_2 and D_3 have to handle reverse voltage given by (2.73). Assuming that the inductor currents have only a very small ripple and the current $i_{n2}(t)$ is almost rectangular, the transistor rms current is found with (2.74). The average forward current of diodes D_2 and D_3 is equal to the output dc current I_{out} . The average forward current of diodes D_1 and D_{11} equals half of the output dc current, since these diodes are connected in parallel. Required power rating of transistors and diodes is found with equations (2.75) to (2.79). Required storage inductances L_1 and L_2 are found with (2.80), while (2.81) gives the effective output capacitance.

$$n = \frac{n_2}{n_1} \quad (2.70)$$

$$M = \frac{1+2 \cdot n}{1-D} \quad (2.71)$$

$$V_{T1(off)} = V_{T11(off)} = V_{D1(R)} = V_{D11(R)} = \frac{1}{1+2 \cdot n} \cdot V_{out} \quad (2.72)$$

$$V_{D2(R)} = V_{D3(R)} = \frac{2 \cdot n}{2 \cdot n + 1} \cdot V_{out} \quad (2.73)$$

$$I_{T1(rms)} \approx \sqrt{(1-D) \cdot \left(\frac{M \cdot I_{out}}{2} + n \cdot \frac{I_{out}}{1-D} \right)^2 + (2 \cdot D - 1) \cdot \left(\frac{M \cdot I_{out}}{2} \right)^2} \quad (2.74)$$

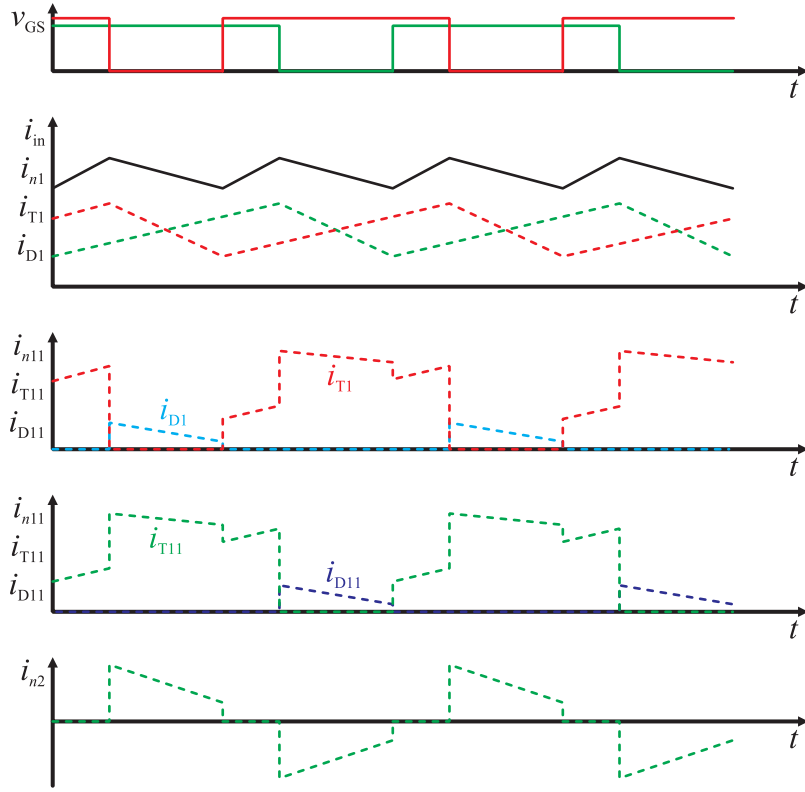


Figure 2.16 Waveforms of the non-isolated two-inductor boost converter

$$\begin{aligned} \text{volt} \times \text{amp}_{T1} &= V_{T1(\text{off})} \cdot I_{T1(\text{rms})} \approx \\ &\approx \frac{1}{2 \cdot n + 1} \cdot \sqrt{\left((1-D) \cdot \left(\frac{M}{2} + \frac{n}{(1-D)} \right)^2 + (2 \cdot D - 1) \cdot \left(\frac{M}{2} \right)^2 \right) \cdot P_{\text{out}}} \end{aligned} \quad (2.75)$$

$$\text{volt} \times \text{amp}_T = 2 \cdot \text{volt} \times \text{amp}_{T1} \quad (2.76)$$

$$\text{volt} \times \text{amp}_{D1} = \frac{1}{2 \cdot n + 1} \cdot V_{\text{out}} \cdot \frac{I_{\text{out}}}{2} = \frac{1}{2 \cdot (2 \cdot n + 1)} \cdot P_{\text{out}} \quad (2.77)$$

$$\text{volt} \times \text{amp}_{D2} = \frac{2 \cdot n}{2 \cdot n + 1} \cdot V_{\text{out}} \cdot I_{\text{out}} = \frac{2 \cdot n}{2 \cdot n + 1} \cdot P_{\text{out}} \quad (2.78)$$

$$\text{volt} \times \text{amp}_D = 2 \cdot (\text{volt} \times \text{amp}_{D1} + \text{volt} \times \text{amp}_{D2}) = \frac{1 + 4 \cdot n}{1 + 2 \cdot n} \cdot P_{\text{out}} \quad (2.79)$$

$$L_1 = L_2 = \frac{V_{\text{in}} \cdot D}{2 \cdot \Delta i_{L1} \cdot f_s} \quad (2.80)$$

$$C_{\text{out}} = \frac{I_{\text{out}} \cdot D}{2 \cdot \Delta v_{\text{out}} \cdot f_s} \quad (2.81)$$

This topology has similar advantages like the non-isolated push-pull-boost converter presented in section 2.2.6. It includes a high voltage gain, reduced

Table 2.1 Component requirements comparison for different dc-dc topologies

	Voltage gain M	Transistors	Diodes	Magnetic components	Capacitors
Basic boost	$\frac{1}{1-D}$	1 HV	1 HV	1 inductor (CCM)	1 HV output
N-phase interleaved boost	$\frac{1}{1-D}$	N HV	N HV	N inductors (DCM or CCM)	1 HV output for N times higher switching freq.
2-phase boost with coupled inductor	$\frac{1}{1-D}$	2 HV	2 HV	1 coupled inductor with $n_2=n_1$	1 HV output for double switching frequency
Cascaded boost	$\frac{1}{1-D_1} \cdot \frac{1}{1-D_2}$	1 LV 1 HV	1 LV 1 HV	1 inductor (CCM) 1 inductor (CCM or DCM)	1 LV intermediate 1 HV output
Center-tapped boost	$\frac{1+n \cdot D}{1-D}$	1 LV	1 LV 1 VHV	1 coupled inductor / flyback transformer with $n_2>n_1$	1 LV snubber 1 HV output
Flyback-boost	$\frac{1+n \cdot D}{1-D}$	1 LV	1 LV 1 VHV	1 coupled inductor / flyback transformer with $n_2>n_1$	2 LV output all series connected
Push-pull-boost	$\frac{1+n}{1-D}$	2 LV	2 LV 2 HV	1 inductor (CCM) 1 push-pull transformer	3 LV output all series connected
Two-inductor-boost	$\frac{1+2 \cdot n}{1-D}$	2 LV	2 LV 2 HV	2 inductors (DCM or CCM) 1 two-winding transformer	3 LV output all series connected

voltage stress on transistors and smooth input current. Moreover this topology utilizes a simple two-winding transformer instead of a more complex three-winding one. Main drawbacks of this topology are several diodes effectively connected in series and three series connected output capacitors.

2.3 Summary

In this chapter the state-of-the-art in non-isolated dc-dc step-up converters has been presented. At the beginning of the chapter different approaches for a dc voltage boosting were introduced. Based on results presented by authors, as well as considering topologies complexity and features it's found that converters with an inductive energy storage are the most suitable ones. They have a fairly low component count and a very good performance among different converter kinds (switched capacitor circuits, resonant, Luo, etc.).

Next, in section 2.2 several different non-isolated step-up topologies were described in details, including diagrams, waveform sketches and key equations.

The survey starts with a well known basic boost converter and guides the reader thru more and more advanced topologies, including coupled inductor topologies. Finally, three topologies derived from isolated dc-dc step-up converters are presented. These are the flyback-boost (known), the push-pull-boost (known) and the two-inductor-boost (new).

Table 2.1 summarizes the voltage gain of considered converters and their component count – separately transistors, diodes, magnetics and capacitors. The knowledge about number of components alone is not enough, so a short description of components is provided too. In the table following abbreviations are used: LV states for a low voltage, i.e. a voltage significantly lower than the output voltage; HV states for a high voltage, i.e. about the output voltage; VHV states for a very high voltage, i.e. a voltage significantly higher than the output voltage. Analyzing the table one can find that the simple topology, like the basic boost converter provides the lowest voltage gain, but it has the fewest parts. Improvement in the voltage gain is done by the price of the component count – it applies to both, passive and active components. The choice of the most suitable topology is not clear yet, especially that only an approximate voltage rating of components is known so far. Analysis and comparison of equations describing converters is not convenient since some of equations are quite complex. Instead, a numerical example is used for a quantitative comparison of components' size.

The example design bases on the specification presented in section 1.4.1. The input voltage is $V_{in}=30$ V, the output voltage is $V_{out}=400$ V and the output power $P_{out}=1000$ W. It's assumed that the efficiency of all converters is 100%. Also no safety margins are taken into account at this point, so absolute minimum values are calculated. The size of the components is expressed in terms of the apparent power or in terms of the average stored energy. Low voltage semiconductors are considered to be below 150 V devices. Moreover, the input current ripple is limited to 20% (peak-peak) of the rated current. The output voltage ripple is 5% (peak-peak) of the dc output voltage. The switching frequency is assumed to be $f_s=50$ kHz basically. Some converters however have more than one transistor operating in phase shift manner. In such case two scenarios are presented for passive components – a) the switching frequency is reduced, so input / output ripples remains at 50 kHz; b) the switching frequency is kept at 50 kHz, so input /output ripple base frequency increases.

The basic boost converter is considered to be a reference topology, since it's the simplest one. This topology has a very poor utilization of the transistor. Paralleling and interleaving of boost converters does not improve it, but interleaving technique enables the reduction of passive components' size, even if the switching frequency is reduced (scenario b). Cascading (series connection) of two or more boost converters improves utilization of transistors. Now, two much smaller transistors are required instead of a large one. Unfortunately, utilization of diodes is degraded and the size of passive components may increase significantly. The center-tapped boost converter and the non-isolated flyback-boost seem to overcome these problems. They ensure a good utilization of the transistor and the diode. Also size of passive components seems to be similar to the basic boost converter. However, these converters have two inherent drawbacks. First, the winding n_2 (see

Table 2.2 Size of components in a 1 kW converter

	Transistors apparent power [VA]	Diodes apparent power [VA]	Energy stored in inductors [mJ]	Energy stored in capacitors [mJ]
Basic boost	12840	1000	45.6	184
2-phase interleaved boost	12840 (2×8420)	1000 (2×500)	a) 42.4 b) 21.2	a) 184 b) 92
4-phase interleaved boost	12848 (4×3212)	1000 (4×250)	a) 34.7 b) 8.7	a) 184 b) 46
2-phase boost with coupled inductor	18148 (2×9074)	1000 (2×500)	a) 46 b) 23	a) 184 b) 92
Cascaded boost (120 V bus)	6268 (3468+2800)	2000 (1000+1000)	72 (37.3+34.7)	290 (150+140)
Center- tapped boost (n=3)	4345	1225 (306+919)	46.2	197.4 (45.4+152)
Flyback- boost (n=3)	4345	1225 (306+919)	46.2	151.2 (45.4+105.8)
Push-pull- boost (n=2)	4816 (2×2408)	1668 (2×167+2×667)	a) 27.3 b) 13.6 1607 VA transf.	a) 243.8 (37.4+2×103.2) b) 121.9 (18.8+2×51.6)
Two- inductor- boost (n=1)	4816 (2×2408)	1668 (2×167+2×667)	a) 54.8 (2×27.4) b) 27.4 (2×13.7) 1333 VA transf.	

Figure 2.9 and Figure 2.12) is not clamped and it resonates with the diode D_2 parasitic capacitance. It results in a huge voltage overshoot across the diode. Second, a huge input current ripple, thus they require an additional input filter. The non-isolated push-pull-boost and the non-isolated two-inductor-boost converters are current fed ones, so input current ripple is limited. Both topologies have a lot in common – they incorporate two low voltage transistors and the voltage doubler rectifiers. Also they offers a good utilization of transistors and stored energy is comparable with the basic boost converter. In the same time these converters provides a very high voltage gain. The non-isolated two-inductor-boost converter offers the highest theoretical voltage gain in this comparison. However one should remember that the turns ratio n definition is slightly different for the push-pull transformer and for the two-winding transformer (equations (2.58) and (2.70)). So, the effective voltage gain in terms for number of turns (not turns ratio) will be similar in both cases.

At this point the non-isolated push-pull-boost seems to be a good candidate for future investigation. First, its good performance is proven [6], while the converter complexity is moderate. Second, this topology has a relatively low requirements in terms of the components rating and it may turn into a compact and cost effective design. Finally, the push-pull transformer can be integrated with the input inductor on a single core, thus the size of the converter can be reduced further (see Chapter 4).

Chapter 3

Power Losses in Dc-Dc Converters

At the beginning of Chapter 2 the assumption of lossless circuits was made. It meant that the output power of the converter equals the input power and no losses are dissipated in the converter. This assumption simplified analysis of converters and helped to develop converter's equations. Unfortunately, in the real world converters are not lossless. The output power of the converter is always lower than the input power and the difference is the power losses dissipated as heat in the converter (3.1). Ratio between the output power and the input power is the power conversion efficiency or just the efficiency (3.2). Knowledge about power losses and heat dissipated in the converter operating under different conditions is critical for a good design and a reliable product. One way to gain this knowledge is to assemble many breadboards and test them intensively. This approach however is very expensive and requires a lot of time. Another way is to use modeling and simulation in the design process.

$$P_{\text{loss}} = P_{\text{in}} - P_{\text{out}} \quad (3.1)$$

$$\eta = \frac{P_{\text{out}}}{P_{\text{in}}} = 1 - \frac{P_{\text{loss}}}{P_{\text{in}}} \quad (3.2)$$

This chapter deals with estimation of power losses in dc-dc non-isolated converters. First a brief overview on different model levels is given and modeling approach is explained. Next, major loss sources are pointed out and suitable loss models are introduced. Finally the presented modeling approach is being applied to the boost converter. Validation of the modeling approach is presented at the end of this chapter.

3.1 Overview on model levels

Nowadays simulation is a widespread and important tool for design and optimization. It is possible to simulate behavior of almost any natural system and power electronics is just one of many applications. To achieve reliable and accurate results it is important to use good models. The question now is what is a good model? The answer is not straightforward at all. Usually the more accurate model is more complex one and requires more computation time. Sometimes however there is no need for a very complex model while a simpler one gives satisfactory results.

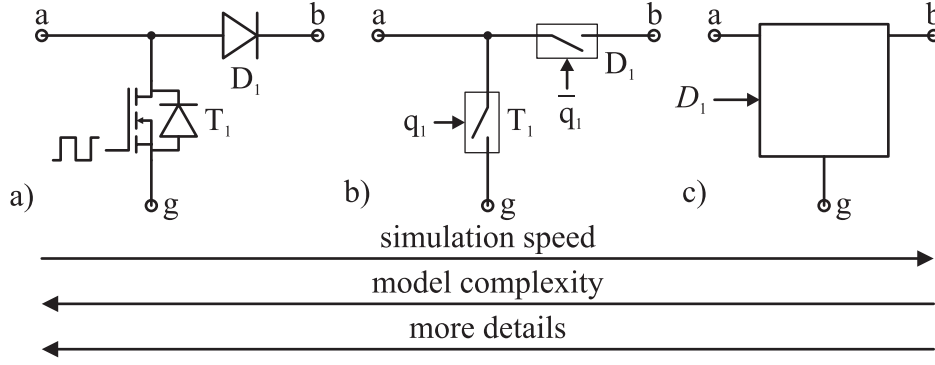


Figure 3.1 Different switching network models - a) a component model; b) an ideal switch model; c) an average model [45]

Figure 3.1 [45] presents three models of the same switching network of a boost converter. Model a) is so called a component model (levels 1 to 5 in [46]). It takes into account many details of the MOSFET and the diode including its switching behavior, thermal characteristics, ageing and so on. Models of this kind are usually very accurate, but they require a lot of computation time. Also these models need many parameters which shall be calculated from a silicon geometry or extracted from measurements.

Model b) is so called an ideal switch model (level 0 in [46]). The MOSFET and the diode are replaced by ideal switches. Sometimes the model has implemented a very basic static characteristic of the component, like on-state resistance or forward voltage drop. Although a dynamic characteristic and other complex phenomena are omitted, it's still possible to observe current and voltage waveforms present in the converter circuit. Thanks to the simpler model and larger time step the simulation speed increases. It's possible to simulate more switching cycles and observe a dynamic behavior of the converter as a whole, which is useful in a control loop design or an operational check of a topology.

Model c) is an average model, which can be considered as a highest level model. Instead of a component models or ideal switches the model is described by averaged functions [47]. All signals are averaged over a switching period and no high frequency variations are taken into account. It doesn't provide a deep insight into the converter's waveforms, but dynamic behavior of the whole converter is being modeled accurately. Computation time is being reduced further. An average model is suitable for a control loop design, simulation of long time periods and analysis of the circuit on a system level.

3.2 Modeling approach

Figure 3.2 presents the diagram of the incorporated model. The model is built up from several interconnected modules, which are organized in a hierarchical structure. The main script runs and supervise the whole loss estimation process. This module can run a simple task, like the power loss calculation in a single operating point. It can perform more complex tasks, like a minimum power loss

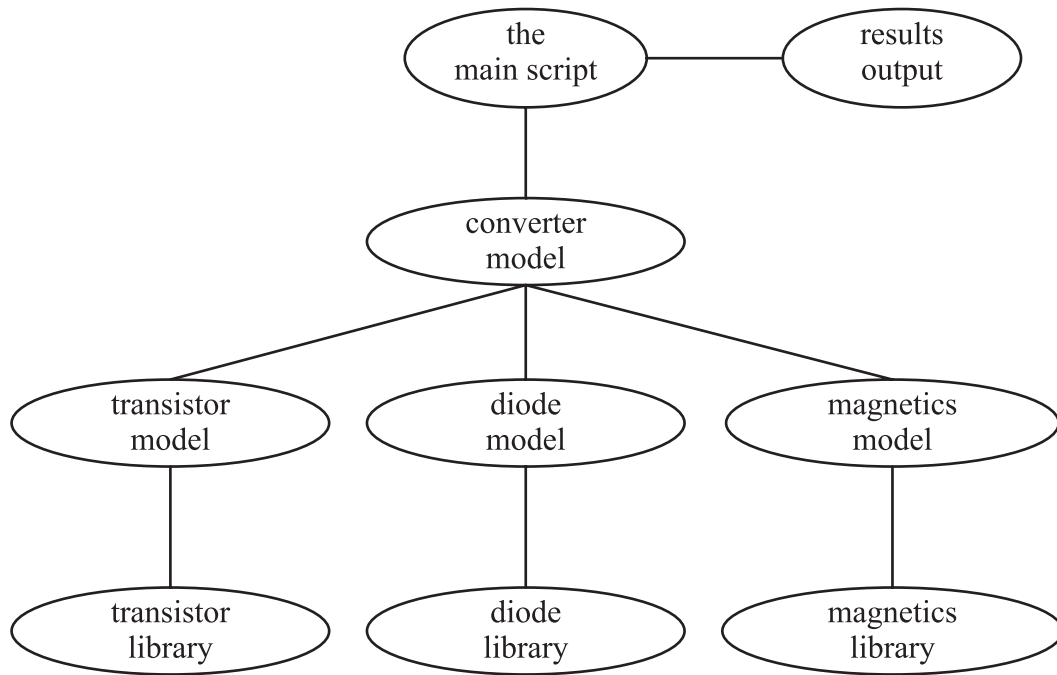


Figure 3.2 The block diagram of the model

search too. The main provides input data about the operating point (the input voltage, the output voltage, the output power etc.) and about used components to the lower level module – the converter model module. The main script collects the loss calculation results and prepares them for the print out.

The converter model's main task is calculation of currents and voltages essential for the power loss calculation by the component models. It includes dc, ac and rms values of currents flowing thru the component. Current and voltage values just before and just after switching are calculated too. Making of a converter model inside a proper circuit simulation software would be the first choice for power loss estimation. Such converter model will base on ideal or detailed component models (level 1 or 2 in [46]), which provide detailed waveforms and accurate results on one hand. On the other hand simulations of several topologies operating under different conditions may take a lot of time. Since power losses are calculated in a steady state it's possible to incorporate a simpler, average model is incorporated. Such a model will provide comparable results in a significantly shorter time. The converter model is built up from the set of equations describing particular currents and voltages, based on the operating point parameters delivered by the main script. In paragraphs 3.2.1 the method for calculation of respective current values is presented.

The component models are responsible for a direct power loss calculation based on values provided by higher level models and component parameters. All considered losses together with relevant equations are described in paragraphs from 3.3 to 3.6. It's important that presented models base on datasheet values in most cases. So, component parameters extraction is vastly reduced or eliminated at all.

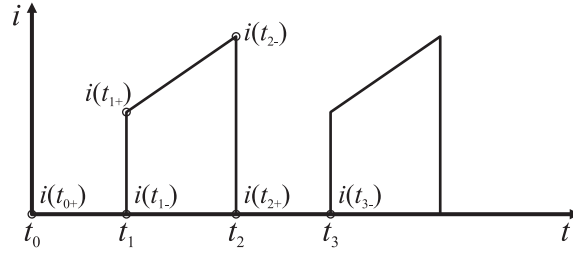


Figure 3.3 Trapezoidal segments

3.2.1 Currents in the circuit

Dc, ac and rms current values are important for estimation of conduction power losses inside components. For estimation of the switching loss knowledge about currents just before and just after switching instant is required. These values can be found easily with a circuit simulator, but it requires a significant amount of computation time. In this paragraph a simple analytical solution is provided.

One can observe that current waveforms of all converters presented in Chapter 2 are composed from trapezoidal segments. Assumption of piecewise linear currents is true for ideal converters only, but it's enough for power losses estimation.

Figure 3.3 presents a simple trapezoidal waveform, similar to a transistor current in a boost converter (Figure 2.2). Finding instantaneous values at the beginning and at the end of each trapezoidal segment allows calculation of dc and rms values according to (3.3) and (3.4). These equations can be generalized ((3.5) and (3.6)) [47]. Then the ac value can be found with (3.8).

$$I = \left(\frac{t_2 - t_1}{t_3 - t_0} \right) \cdot \left(\frac{i(t_{2-}) + i(t_{1+})}{2} \right) \quad (3.3)$$

$$I_{(rms)} = \sqrt{\left(\frac{t_2 - t_1}{t_3 - t_0} \right) \cdot \frac{1}{3} \cdot \left(i(t_{1+})^2 + i(t_{1+}) \cdot i(t_{2-}) + i(t_{2-})^2 \right)} \quad (3.4)$$

$$I = \sum_{k=1}^n \left(\frac{t_k - t_{k-1}}{t_n - t_0} \right) \cdot \left(\frac{i(t_{k-}) + i(t_{(k-1)+})}{2} \right) \quad (3.5)$$

$$I_{(rms)} = \sqrt{\sum_{k=1}^n \left(\frac{t_k - t_{k-1}}{t_n - t_0} \right) \cdot u_k} \quad (3.6)$$

$$u_k = \frac{1}{3} \cdot \left(i(t_{(k-1)+})^2 + i(t_{(k-1)+}) \cdot i(t_{k-}) + i(t_{k-})^2 \right) \quad (3.7)$$

$$I_{(ac)} = \sqrt{I_{(rms)}^2 - I^2} \quad (3.8)$$

In the same way all current waveforms are analyzed and respective equations in MATLAB® format are presented in Appendix B.

3.3 Transistor

Majority of power transistors used in power electronic converters are IGBTs and Power MOSFETs (referred here as MOSFETs). IGBTs are desired for high power applications. They handle voltages exceeding 600-1000 V and currents much greater than 100 A. The price for it is a poor switching performance, thus IGBTs' switching frequency is limited. On the other hand in applications where voltages do not exceed 600 V MOSFETs are preferred because of its fast switching and relatively low conduction losses. This section deals with power losses present in a MOSFET transistors. Two major sources are recognized: a conduction loss and switching losses. Further total switching losses break up into turn-on, turn-off, gate and reverse recovery losses. However the term switching loss used in following sections refers to turn-on and turn-off losses only. The reverse recovery loss is caused by the diode reverse recovery phenomena and it is discussed in section 3.4.2.

3.3.1 Conduction loss

MOSFET conduction loss, also called on-state loss, is caused by the current flowing thru the transistor's internal resistance (channel resistance) $R_{DS(on)}$ and it's simply described by (3.9). The transistor rms current $I_{T(rms)}$ is found by analysis of converter current waveforms. The transistor rms current of selected topologies are presented in Chapter 2. On-state resistance $R_{DS(on)}$ is published in datasheets while it's a basic parameter of any MOSFET. In the transistor operating in the ohmic region (also called the on-state region) the resistance $R_{DS(on)}$ practically depends only on the junction temperature T_j . Actual on-state resistance $R_{DS(on)}$ for given junction temperature T_j are read from datasheet plots. For simulation purposes resistance-temperature relationship is approximated by (3.10). Term $R_{DS(on)25}$ is the on-state resistance at the junction temperature of 25°C and $r_{DS(on)T}$ is the temperature coefficient of the resistance.

$$P_{Tcond} = R_{DS(on)} \cdot I_{T(rms)}^2 \quad (3.9)$$

$$R_{DS(on)} = R_{DS(on)25} + (T_j - 25^\circ\text{C}) \cdot r_{DS(on)T} \quad (3.10)$$

3.3.2 Switching loss

Estimation of turn-on and turn-off losses is not that simple. Switching of a MOSFET is a complex process, which depends on operating conditions and the converter topology. In the literature [43, 47-50] one can find more or less detailed descriptions of the MOSFET switching. However mathematical description of the switching loss is often limited to a very general equation (3.11). Gate controlled switching of an inductive clamped load is assumed here. This kind of switching is true for all converters presented in Chapter 2. Figure 3.4 shows the MOSFET with its parasitic capacitances placed in the equivalent switching circuit. Equations (3.12), (3.13) and (3.14) define the input capacitance C_{iss} , the output capacitance C_{oss} and the reverse transfer capacitance C_{rss} . Capacitances C_{oss} and C_{rss} are strongly variable with the drain-source voltage (here referred as $v_T(t)$). The current source I_l represents the inductor current, which is considered to be constant during switching.

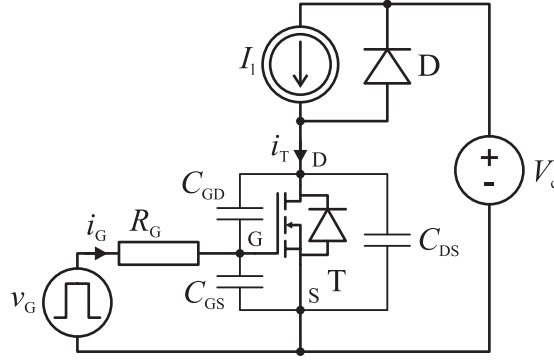


Figure 3.4 A clamped inductive load switching circuit and parasitic capacitances of the MOSFET

The voltage source V_c represents the capacitor voltage (the clamping voltage) and it's also constant during switching. The diode D is assumed to be an ideal one, so no reverse recovery and no forward recovery is taken into account at this point. The MOSFET is controlled by the square-wave voltage v_G , which is V_G either zero. The gate current $i_G(t)$ is limited by the gate resistor R_G .

$$P_{Tsw} = f_s \cdot \int_{\text{switching transitions}} v_T(t) \cdot i_T(t) dt \quad (3.11)$$

$$C_{iss} = C_{GS} + C_{GD} \quad (3.12)$$

$$C_{oss} = C_{DS} + C_{GD} \quad (3.13)$$

$$C_{rss} = C_{GD} \quad (3.14)$$

The gate controlled switching has several stages like presented on Figure 3.5. From the switching power loss point of view only four stages are important. Those are:

- t_1-t_2 – called current rise time t_{ir} , during this period the drain current $i_T(t)$ linearly increases from zero to the load current I_l , the drain-source voltage $v_T(t)$ remains almost constant at the clamping voltage level V_c
- t_2-t_3 – called voltage fall time t_{vf} , during this period the drain-source voltage $v_T(t)$ falls from the clamping level V_c to the on-state voltage $R_{DS(on)} \cdot I_l$, this voltage transition is strongly non-linear
- t_6-t_7 – called voltage rise time t_{vr} , during this period the drain-source voltage $v_T(t)$ rises from the on-state voltage to the clamping voltage V_c , also this voltage transition is non-linear
- t_7-t_8 – called current fall time t_{if} , during this period the drain current $i_T(t)$ linearly falls from the load current level I_l to zero

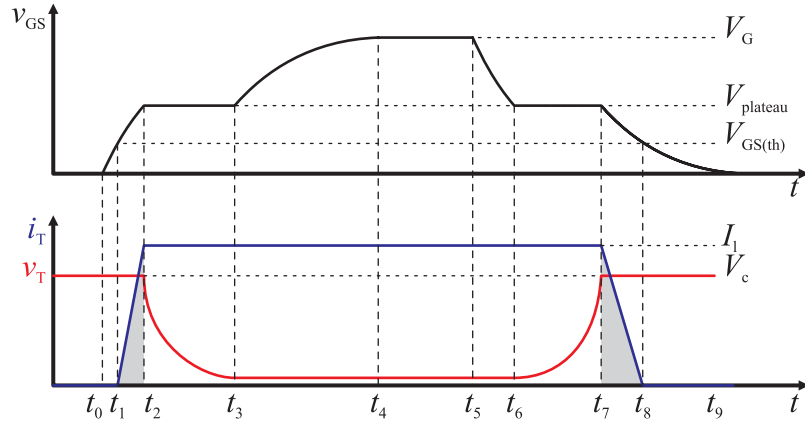


Figure 3.5 MOSFET switching waveforms

The total energy dissipated during turn-on and turn-off is expressed as the sum of energy portions (3.15) dissipated during four stages mentioned above. Energy dissipated during current rise time and current fall time is given by (3.16) and (3.17). It's simply calculated as the area of gray triangles from Figure 3.5 since the drain current rises and falls in almost linear manner and the drain-source voltage remains constant. Current rise time t_{ir} is found by analysis of the gate circuit and the gate-source voltage $v_{GS}(t)$ [48]. After the voltage V_G is applied to the gate circuit the gate-source voltage $v_{GS}(t)$ increases. Once the voltage $v_{GS}(t)$ reaches the threshold level $V_{GS(th)}$ the drain current $i_D(t)$ starts to rise. The transistor is in its active region, so the gate-source voltage $v_{GS}(t)$ and the drain current $i_D(t)$ are coupled together by the transconductance g_{fm} . The gate-source voltage rises to the plateau voltage $V_{plateau}$ given by (3.20). In the same time the drain current reaches the load current level I_l and the current transition is done. The gate circuit is basically a RC circuit driven by the square-wave voltage $v_G(t)$, so the current rise time t_{ir} is found as time required by the gate-source voltage $v_{GS}(t)$ to increase from the threshold level $V_{GS(th)}$ to the plateau voltage $V_{plateau}$ (3.18). Current fall time t_{if} is found in similar way. The gate circuit is discharged and the gate-source $v_{GS}(t)$ decreases from the plateau voltage $V_{plateau}$ to the threshold voltage $V_{GS(th)}$ (3.19).

$$P_{Tsw} = f_s \cdot (W_{ir} + W_{vf} + W_{vr} + W_{if}) \quad (3.15)$$

$$W_{ir} = t_{ir} \cdot I_l \cdot V_c \quad (3.16)$$

$$W_{if} = t_{if} \cdot I_l \cdot V_c \quad (3.17)$$

$$t_{ir} = R_G \cdot C_{iss} \cdot \ln \left(\frac{V_G - V_{GS(th)}}{V_G - V_{plateau}} \right) \quad (3.18)$$

$$t_{if} = R_G \cdot C_{iss} \cdot \ln \left(\frac{V_{plateau}}{V_{GS(th)}} \right) \quad (3.19)$$

$$V_{plateau} = V_{GS(th)} + \frac{I_l}{g_{fm}} \quad (3.20)$$

Estimation of energy dissipation during voltage rise and voltage fall requires more sophisticated approach because of non-linear voltage transitions. During these phases the gate-source voltage v_{GS} is constant as stated before. This fact has two important implications. First, the gate current i_G is constant and it's easy to find with (3.21), assuming that $v_{GS}(t)=V_G$ during turn-on transition and $v_{GS}(t)=0$ during turn-off transition. Second, the gate current $i_G(t)$ charges or discharges the C_{rss} capacitance only. Since $V_{plateau} \ll V_c$ the slope of $v_{GD}(t)$ is about the same like the slope of $v_T(t)$ (3.22), which makes analysis of $v_T(t)$ easier [50]. The range of $v_T(t)$ and $v_{GD}(t)$ variation is divided into n discrete steps. Next, (3.23) is used to find the time t_k required to increase or decrease the voltage $v_T(t)$ from one discrete value $v_T(k)$ to the other discrete value $v_T(k+1)$. For each step value of C_{rss} is updated in respect to the actual $v_T(k)$ voltage. Finally energy dissipated during voltage fall time is found as a sum of energy portions dissipated in each step (3.24). In the same way energy dissipated during voltage rise time is found.

$$i_G(t) = \frac{v_{GS}(t) - V_{plateau}}{R_G} \quad (3.21)$$

$$\frac{dv_T(t)}{dt} \approx \frac{dv_{GD}(t)}{dt} \quad (3.22)$$

$$t_k = C_{rss}(v_T(k)) \cdot \frac{v_T(k+1) - v_T(k)}{i_G(t)} \quad (3.23)$$

$$W_{vf} = \sum_{k=0}^n t_k \cdot v_T(k) \cdot I_1 \quad (3.24)$$

3.3.3 Gate loss

Gate loss comes from charging and discharging the MOSFET input capacitance C_{iss} thru the gate resistor R_G and it's given by (3.25). Term Q_G is the gate total charge which is available in datasheets. Most of this energy is dissipated in the external gate resistor and the driver. Portion of this energy might be dissipated inside the MOSFET if there is any significant internal gate resistance.

$$P_{Tgate} = f_s \cdot Q_G \cdot V_G \quad (3.25)$$

3.4 Diode

Next to a transistor, a diode is a key semiconductor component. Fast switching of the diode has the same importance like a low conduction loss. Schottky diodes provide outstanding switching performance and a low conduction loss in the same time, but the blocking voltage is limited to 150-200 V. Fast silicon (pn-junction) diodes have been used if higher blocking voltage is required. Despite a great technology improvement done during years the reverse recovery behavior remained the main drawback of silicon diodes. Recent development in wide bandgap semiconductor materials (SiC, GaN and similar) enabled mass production of next

generation high voltage Schottky diodes, which overcome reverse recovery problem. Following sections describe estimation of different losses present in power diodes.

3.4.1 Conduction loss

Forward characteristic of a power diode is non-linear and it's presented on Figure 3.6. For simulation purposes a linear approximation is used. It includes the forward voltage drop $V_{D(F)}$ and the forward resistance R_F . This simple model is sufficient for the conduction loss calculation according to (3.26). Sometimes the diode rms current $I_{D(rms)}$ is replaced by the diode average current I_D for sake of simplicity. However if the ac component of the diode current is significant then the diode rms current shall be used. Also one shall remember that both, the forward voltage drop $V_{D(F)}$ and the forward resistance R_F are temperature dependent ((3.27) and (3.28)). All required diode parameters are extracted from forward characteristic plots available in datasheets.

$$P_{Dcond} = V_{D(F)} \cdot I_D + R_F \cdot I_{F(rms)}^2 \quad (3.26)$$

$$R_F = R_{F25} + (T_j - 25^\circ C) \cdot r_{FT} \quad (3.27)$$

$$V_{D(F)} = V_{D(25)} + (T_j - 25^\circ C) \cdot v_{D(T)} \quad (3.28)$$

3.4.2 Reverse recovery loss

The reverse recovery (or diode turn-off) behavior of a silicon power diode is considered as the most important for the circuit performance, while it may lead to severe losses in the transistor and the diode itself. Switching of an inductive clamped load is assumed. The switching circuit and related switching waveforms are presented on Figure 3.9 and Figure 3.7. When the transistor is turned-on the load current I_l is being commutated from the diode to the transistor. The diode current fall rate $di(t)/dt$ may exceed 1000 A/ μ s in many cases, but the pn-junction diode will not move from conduction to blocking state immediately. The stored

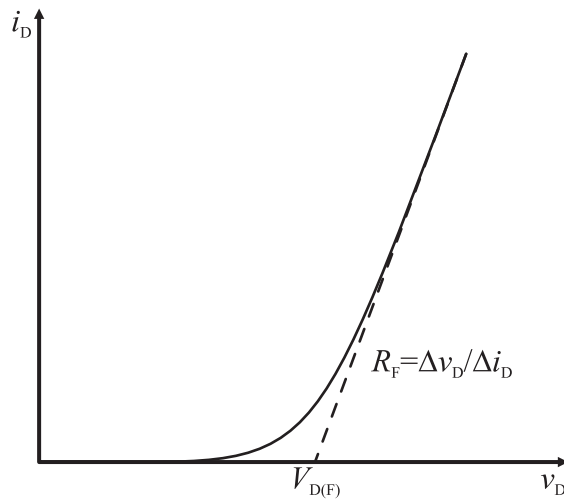


Figure 3.6 Forward characteristic of a diode and its linearization

charge has to be removed from the junction vicinity before the diode can block the reverse voltage. It results in the reverse current $i_D(t)$ flowing thru the diode D, the transistor T and the clamping voltage source V_c . Exact shape of the diode reverse current depends on many factors, where the most important are: the diode material and manufacturing technology, the junction temperature, the diode current fall rate $di(t)/dt$. In the literature one can find several physical diode models suitable for the reverse recovery loss calculation [51, 52].

Majority of the reverse recovery power loss is dissipated in the transistor commutating with the diode. A simple and robust method for calculation of this loss is described in [47]. The method is valid if the time t_f is significantly less than the time t_s (see Figure 3.7), which is true for a low softness factor s (3.29) or so called “snappy” diodes. Additional power P_{Tr} dissipated in the transistor is simply described by (3.30) [47]. Values of the reverse recovery time t_{rr} and the reverse recovery charge Q_{rr} are found in datasheet plots as a function of the diode current slope $di(t)/dt$. The diode current slope $di(t)/dt$ is determined either by the transistor gate driver (the transistor current rise time t_{tr}), or by the clamping voltage and stray inductances present in the circuit – whichever gives lower $di(t)/dt$.

$$s = \frac{t_f}{t_s} \quad (3.29)$$

$$P_{Tr} = f_s \cdot (V_c \cdot I_l \cdot t_{rr} + V_c \cdot Q_{rr}) \quad (3.30)$$

Some energy is dissipated in the diode during its turn-off too. For “snappy” diodes this is a very small loss and usually is neglected. However in case of soft recovery diodes (a large softness factor s) it should be taken into account [53]. Assuming linear voltage and current transitions in the diode the power dissipated in

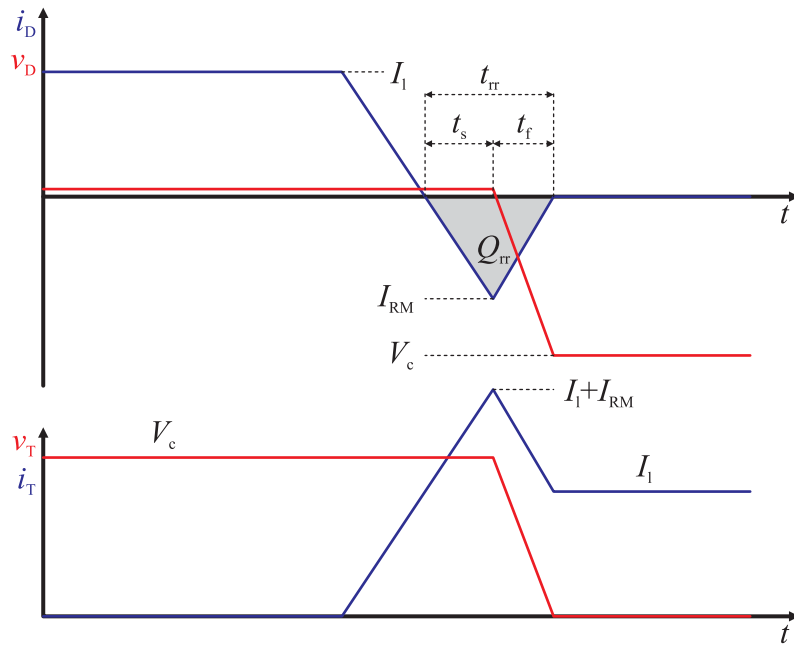


Figure 3.7 Reverse recovery of a pn-junction silicon diode diode waveforms (top) and transistor waveforms (bottom)

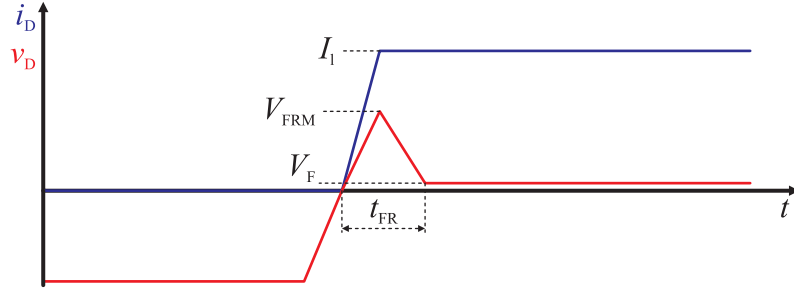


Figure 3.8 Forward recovery of a diode

the diode is given by (3.31). The time t_f is found with (3.32) by rearranging (3.29), while the softness factor s and the reverse recovery time t_{rr} are available in datasheets.

$$P_{\text{Doff}} = f_s \cdot (t_f \cdot I_{\text{RM}} \cdot V_c) \quad (3.31)$$

$$t_f = \frac{s \cdot t_{rr}}{s + 1} \quad (3.32)$$

3.4.3 Forward recovery

The diode waveforms during its turn-on are presented on Figure 3.8. When the diode passes from the blocking state to the conduction state the forward voltage temporary increases to the peak forward voltage V_{FRM} before it drops to the steady-state forward voltage $V_{\text{D(F)}}$. During fast switching the peak forward voltage V_{FRM} may exceed 100 V in some cases. This voltage adds to the transistor turn-off voltage and it has two important results. First, it creates voltage overshoot across the transistor and may lead to the device failure. Second, the increased turn-off voltage of the transistor may cause increased switching loss during its turn-off. Forward recovery and the peak forward voltage V_{FRM} causes power loss P_{Don} in the diode. Using linear approximation of waveforms, like presented in [53], this power is found with (3.33). This simplified method assumes that the diode current rise time is very short in compare to the forward recovery time t_{fr} of the diode, so the current i_A is almost rectangular. This assumption often leads to overestimation of actual turn-on energy in the diode. Since this energy loss is fairly small in compare to conduction loss and turn-off loss it's often neglected.

$$P_{\text{Don}} = f_s \cdot (t_{fr} \cdot I_1 \cdot V_{\text{FRM}}) \quad (3.33)$$

3.4.4 Capacitive loss

Figure 3.9 presents a clamped inductive load switching circuit and the diode capacitance C_D is marked. During the converter operation this capacitance is charged and discharged periodically. During diode turn-on energy stored in the diode capacitance is lost [47]. In the simplest form the capacitive loss P_{Dcap} is described by (3.34). The estimation is not trivial since the diode capacitance C_D is a function of the reverse voltage $v_{\text{D(R)}}(t)$. The range of the reverse voltage variation (from $-V_c$ to 0) is divided into n discrete steps. Then the actual value of the diode

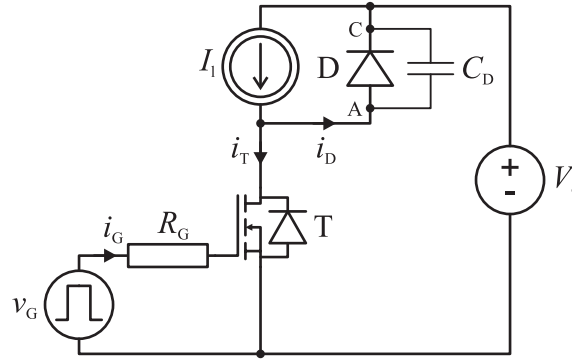


Figure 3.9 A clamped inductive load switching circuit and parasitic capacitance of the diode

capacitance C_D is found from the datasheet plot for each voltage step. The total charge stored in the diode capacitance is calculated as a sum of small charges for each voltage step (3.35).

$$P_{\text{Dcap}} = f_s \cdot \left(\frac{1}{2} \cdot Q_D \cdot V_c \right) \quad (3.34)$$

$$Q_D = \sum_{k=1}^n C_D \left(v_{D(R)}(k) \right) \cdot \left(v_{D(R)}(k+1) - v_{D(R)}(k) \right) \quad (3.35)$$

When pn-junction silicon diode is used the capacitive loss is often neglected since it's small in compare to other loss components, especially in compare to reverse recovery loss. However if a Schottky diode is used then the capacitive loss should be taken into account. It's because a Schottky diode has larger capacitance and it has no reverse recovery loss. So, the capacitive loss become larger and visible among other loss components.

3.5 Magnetic device

Magnetic components are very important parts of any power converter. In many cases they are designed especially for the particular converter, rather than selected among available off-the-shelf parts. Core loss and copper loss are two major loss sources in magnetic devices regardless it's type and design details. Following sections describe these losses, modeling of them and their impact on particular magnetic devices like an inductor, a transformer or a flyback transformer.

3.5.1 Copper loss

The copper loss is one of two loss mechanisms present in most of magnetic devices. Basically it's caused by the current flowing thru the winding, whose resistance is non-zero. So called the low frequency copper loss is expressed by well known equation (3.36), where I_{rms} is the rms value of the current and R is the low frequency resistance given by (3.37). The low frequency resistance bases only on the wire cross section area A_{Cu} , the wire length l_{Cu} and its resistivity ρ . It

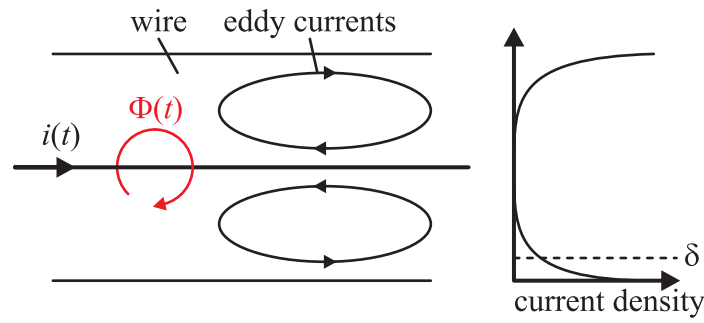


Figure 3.10 Skin effect

doesn't include any high frequency effects. In a switch mode converter operating in kilohertz or megahertz range the low frequency approach limits to the dc current components only. The equation (3.36) become (3.38) in such case.

$$P_{Cu} = R \cdot I_{(rms)}^2 \quad (3.36)$$

$$R_{dc} = \frac{\rho \cdot l_{Cu}}{A_{Cu}} \quad (3.37)$$

$$P_{Cude} = R_{dc} \cdot I^2 \quad (3.38)$$

Estimation of the ac copper loss requires a more sophisticated approach. Basically the ac copper loss is expressed by (3.39), similarly to the dc copper loss. However at high frequency the winding resistance increase is observed ($R_{ac} > R_{dc}$). The resistance increase is basically caused by eddy currents inside the winding conductor – the most pronounced phenomenas responsible for eddy currents are the skin effect and the proximity effect. Both phenomenas are widely described in the literature [43, 47, 54-62], so here only a brief explanation is given together with a simple method for estimation of the ac copper loss.

$$P_{Cuac} = R_{ac} \cdot I_{ac}^2 \quad (3.39)$$

The skin effect is explained using Figure 3.10 [47]. There is the non-magnetic wire conducting the high frequency current $i(t)$. The current $i(t)$ induces the magnetic flux $\Phi(t)$. According to Lenz's law the ac flux $\Phi(t)$ induced current (eddy currents) inside the wire. These eddy currents tend to oppose the ac flux and flow in the manner presented on Figure 3.10. Eddy currents add to the main current $i(t)$ and it results in a non-uniform current density inside the wire. The high frequency current $i(t)$ do not penetrate to the center of the wire, but flows on the surface of the wire. Because the center of the wire is not utilized, the effective wire cross section are is reduced thus the ac resistance increases over the dc resistance given by (3.37). The ac resistance R_{ac} of a single wire is given by (3.40), where δ is so called penetration depth and h is the wire thickness. The penetration depth is given by (3.41), where f is the current frequency, ρ is the wire resistivity and μ is the magnetic permeability of the wire (in most cases $\mu = \mu_0$).

$$R_{ac} = \frac{h}{\delta} \cdot R_{dc} \quad (3.40)$$

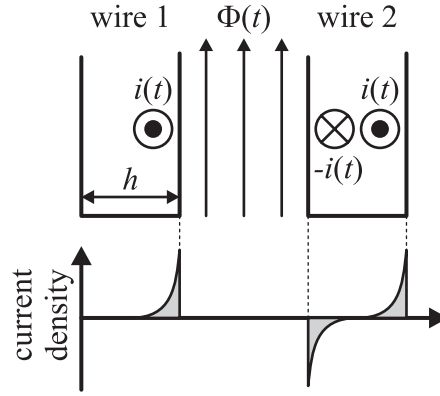


Figure 3.11 Proximity effect

$$\delta = \sqrt{\frac{\rho}{\pi \cdot \mu \cdot f}} \quad (3.41)$$

The proximity effect is shortly explained using Figure 3.11 [47]. There are two parallel wires in a close proximity. The wire 1 carries the high frequency current $i(t)$, while the wire 2 is open circuit and its net current is zero. The penetration depth δ is significantly smaller than the wires thickness h . Now, the current $i(t)$ generates the flux $\Phi(t)$ around the wire 1. The flux attempts to penetrate the wire 2 and by Lenz's law current is induced in the wire 2. Because the wire 2 is open circuit the induced current path has to close inside the wire 2 – the current flows in one direction on the left side of the wire 2 and in the opposite direction on the right side, like presented on Figure 3.11. In a multilayer designs the proximity effect may lead to a severe ac copper loss.

In the literature one may find different methods for estimation of the ac resistance and the related ac copper loss [43, 47, 54-62]. Some of these methods base on Dowell's work and one dimensional (1D) approach, while some other incorporate more complex two dimensional (2D) approach. Here the simple method for estimation of the ac losses is presented [47]. The method bases on 1D approach and it is intended and suitable for analysis of windings made out of a uniform foil of the thickness h . It's possible to extend the method to windings made out of a square wire and a round wire. In this method the resistance factor F_R binding the dc resistance R_{dc} and the ac resistance R_{ac} is used. The resistance factor F_R is found based on the winding geometry (number of layers m , the layer thickness h , penetration depth δ etc.) with (3.42), where φ is the relative penetration depth given by (3.43) (for foil windings). Functions $G_1(\varphi)$ and $G_2(\varphi)$ are given by (3.44) and (3.45) respectively. Solving (3.42) for M -layer design leads to (3.46), which is plotted on Figure 3.12.

$$F_R = \frac{R_{ac}}{R_{dc}} = \frac{1}{M} \sum_{m=1}^M \varphi \cdot (2 \cdot m^2 - 2 \cdot m + 1) \cdot G_1(\varphi) - 4 \cdot m \cdot (m-1) \cdot G_2(\varphi) \quad (3.42)$$

$$\varphi = \frac{h}{\delta} \quad (3.43)$$

$$G_1(\varphi) = \frac{\sinh(2 \cdot \varphi) + \sin(2 \cdot \varphi)}{\cosh(2 \cdot \varphi) - \cos(2 \cdot \varphi)} \quad (3.44)$$

$$G_2(\varphi) = \frac{\sinh(\varphi) \cdot \cos(\varphi) + \cosh(\varphi) \cdot \sin(\varphi)}{\cosh(2 \cdot \varphi) - \cos(2 \cdot \varphi)} \quad (3.45)$$

$$F_R = \varphi \left[G_1(\varphi) + \frac{2}{3} \cdot (M^2 - 1) \cdot (G_1(\varphi) - 2 \cdot G_2(\varphi)) \right] \quad (3.46)$$

As mentioned above, the method can be extended for a windings made out of a round wire filling the whole core window width. For that purpose the relative penetration depth φ given by (3.43) is replaced by the one given by (3.47). The coefficient η is so called porosity factor. It's defined as the ratio between the actual layer copper area to the area of the effective foil conductor (3.48). For round wires that span the bobbin the typical value of η is 0.8. As presented on Figure 3.12 a large ac copper loss occurs for a large number of layers m and a large relative penetration depth φ . So, the general guideline is to avoid multilayer designs, to use the interleaved windings whenever possible [43, 47, 59] and to keep the layer thickness below the penetration depth ($h < \delta$). The method does not include presence of the air gap, the edge effects and it's not valid for complex or non-uniform winding configurations (e.g. arranged on a toroidal core).

$$\varphi = \sqrt{\eta} \cdot \sqrt{\frac{\pi}{4}} \cdot \frac{d}{\delta} \quad (3.47)$$

$$\eta = \frac{A_{\text{Cu round}}}{A_{\text{Cu foil}}} \quad (3.48)$$

The analysis above is valid for sinusoidal currents, which are rare in switch mode

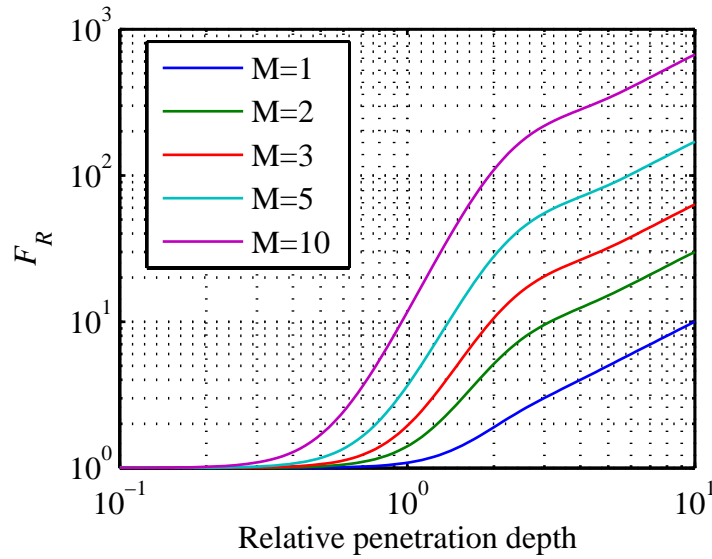


Figure 3.12 The resistance factor F_R as a function of the relative penetration depth φ and the number of layers M

converters. Typical current waveform is far from being sinusoidal and it contains a significant harmonic content. Such current waveform is expressed using Fourier series and the ac copper loss is calculated for each harmonic separately [47, 59].

Nowadays, thanks to the increasing processing power of desktop computers 2D and 3D finite element methods (FEM) are used for design and optimization of magnetic devices. FEM approach provides a very good accuracy and enables analysis of any complex winding and core configuration. It enables automated harmonic analysis of arbitrary current waveform too.

3.5.2 Core loss

The core loss is the second loss mechanism present in most of magnetic devices. It's commonly accepted that the core loss is caused by two physical effects – the hysteresis of the material and eddy currents inside the core [47]. Not all energy required to change the magnetization of the core can be recovered. Part of this energy is lost inside the core as a heat and electrically observed as a hysteresis loop. Because the core is a better or worse conductor placed in a variable magnetic field eddy currents flow inside the core. Both phenomenas contribute to the total core loss.

Over the years several different methods and modeling approaches were presented. Reference [63] points out most common approaches for modeling of the core loss: the hysteresis models (Jiles-Atherton model and Preisach model), the loss separation model and the empirical model (Steinmetz equation). Reference [64] gives a good insight into magnetization process of ferrites bases on domains (domain walls) hypothesis. Also it states that the only origin of losses are eddy currents around moving domain walls. However even detailed knowledge about physical origin of the core doesn't provide necessary practical method for calculation of the core loss. So far the method based on the work done by Steinmetz is widely used. The foundation of the method is so called Steinmetz equation (3.49).

$$p_{Fe} = k \cdot f^{\alpha} \cdot \Delta B^{\beta} \quad (3.49)$$

This empirical equation states that the specific core loss (loss per volume unit) is a function of the magnetization frequency f and the flux density amplitude ΔB . Parameters k , α and β are determined experimentally and they are commonly found in core datasheets. Simple and robust Steinmetz equation together with parameters available for different materials (ferrites, powders) makes this method very popular and ready to use. However three main drawbacks of this method are recognized. First, parameters (k , α , β) published in datasheets are valid only for sinusoidal excitation. It makes the method inaccurate for switch mode converters, while the magnetic flux in the core is not sinusoidal. Second, the basic Steinmetz equation doesn't include any dc bias influence. It may lead to miscalculation of the core loss in case of dc inductors or flyback transformers. Finally, the method doesn't include temperature changes, so it's valid and accurate for one temperature only. Usually parameters k , α and β are given for 100°C, which is close to the operating temperature of many magnetic components.

To overcome non-sinusoidal flux problem several methods were introduced [63, 65-68]. So called modified Steinmetz equation (MSE) seems to be robust and efficient method [63]. This method doesn't require any additional parameters beyond Steinmetz equation coefficients k , α and β . The method bases on the fact, that the core loss is a function of the magnetization rate rather than the switching frequency alone. MSE is given by (3.50), where f_r is the repetition frequency, f_{eq} is so called equivalent frequency. The repetition frequency f_r in a switch mode converter equals the switching frequency. The equivalent frequency f_{eq} is defined as the frequency of the sinusoidal flux density, whose has the same flux density amplitude ΔB and the same average magnetization rate like the considered arbitrary flux density waveform. For a piecewise linear flux density waveform the equivalent frequency is given by (3.51).

$$p_{Fe} = (k \cdot f_{eq}^{\alpha-1} \cdot \Delta B^\beta) \cdot f_r \quad (3.50)$$

$$f_{eq} = \frac{2}{\pi^2} \cdot \sum_{k=2}^K \left(\frac{B_k - B_{k-1}}{2 \cdot \Delta B} \right)^2 \cdot \frac{1}{t_k - t_{k-1}} \quad (3.51)$$

Influence of the dc bias (premagnetization) on the core loss is discussed in literature and several authors reported an increased core loss under dc bias conditions [63, 69, 70]. Estimation of such a loss is difficult, mainly due to lack of data from manufacturers and lack of a robust, widely accepted model. In [63] a simple extension of Steinmetz equation is proposed. In this method the parameter k from Steinmetz equation (3.49) is replaced by new parameter k' given by (3.52). The new parameter depends on both dc and ac components of the flux density. It also utilizes two new parameters K_1 and K_2 which are extracted for each ferrite material, since they are not provided by manufacturers so far.

$$k' = k \cdot \left(1 + K_1 \cdot B_{dc} \cdot e^{\left(\frac{\Delta B}{K_2} \right)} \right) \quad (3.52)$$

Analysis of a ferrite datasheet shows that the core loss is a strong function of the core temperature. I.e. the popular power ferrite material 3F3 operating at 100 kHz and 100 mT has the specific core loss 170 mW/cm³ in room temperature (20 °C). Under the conditions (frequency and flux density), but in operating temperature of 100 °C the specific core loss goes down to about 70 mW/cm³ [71]. In the same datasheet Steinmetz equation parameters are given for operating temperature of 100 °C only. So, estimation of the core loss based on Steinmetz equation only may lead to significant errors if the operating temperature differs from 100 °C (e.g. during the converter warm-up period). To overcome this problem a simple extension of Steinmetz equation is proposed in [65] and it's given by (3.53). It simply includes parabolic correlation between the core loss and the temperature T . Parameters ct_2 , ct_1 and ct have to be extracted experimentally or from the datasheet for the core material. Moreover these parameters are the flux density and the frequency dependent in most cases. So, similarly to Steinmetz equation parameters they are valid only for the certain frequency/flux density range.

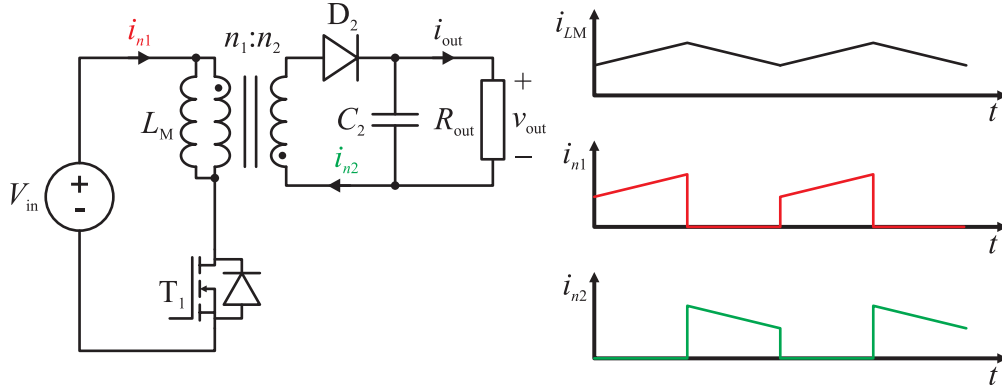


Figure 3.13 The flyback converter and the flyback transformer currents

$$p_{Fe} = k \cdot f^\alpha \cdot \Delta B^\beta \cdot (ct_2 \cdot T^2 - ct_1 \cdot T + ct) \quad (3.53)$$

Even in spite of these limitation Steinmetz equation proves to be a very robust and fairly sufficient method for the core loss preliminary estimation. More accurate results, by the cost of computation time, are obtained with a combined hysteresis-FEM models [72].

3.5.3 Types of magnetic devices and their losses

Various kinds of magnetic devices are used in power electronics. Depending on the kind of the magnetic device core and copper losses might be balanced or one of them can be dominant. In this section losses in magnetic components of non-isolated dc-dc converters are discussed and the focus is on converters presented in Chapter 2. It includes a dc inductor, a flyback transformer and a high frequency transformer.

A dc inductor is a storage element, so it utilizes an air gap to store energy. For a constant permeability μ the flux density $B(t)$ is directly proportional to the current $i_L(t)$ (3.54), so a small current ripple Δi_L indicates a small ac flux density component ΔB . In case of a gapped ferrite core it means a very low core loss, so it's most likely so called saturation limited design (powder cores however may still exhibit a considerable core loss). Also a very small ac current ensures a fairly low ac copper loss, even if the ac resistance is much larger than the dc resistance of the winding. In a dc inductor design dc copper loss is dominant. In case of an inductor current with a larger ac component (e.g. close to DCM) the ac copper loss may become significant very quickly, so the ac resistance become an important constraint.

$$B(t) = \frac{\mu \cdot n \cdot i_L(t)}{l_g} \quad (3.54)$$

A flyback transformer, similarly to the dc inductor, stores energy in an air gap. The difference is that the flyback transformer uses one winding to store energy (e.g. winding n_1) and another to release energy (e.g. winding n_2). The equivalent circuit and relevant waveforms are presented on Figure 3.13. The inductor L_M represents the magnetizing inductance referred to the primary winding n_1 . Assuming a

constant permeability the flux density $B(t)$ is directly proportional to the magnetizing current $i_{LM}(t)$ – by analogy to (3.54). Now, the ac flux density ΔB may remain small, so the core loss is small too. But both winding currents $i_{n1}(t)$ and $i_{n2}(t)$ contain a large dc and ac components, since they are discontinuous. In a flyback transformer design the focus is on reduction of both, dc and ac winding resistances.

A transformer contrary to the flyback transformer doesn't store energy and it utilizes an ungapped ferrite core having a very high permeability μ . Now, the flux density $B(t)$ is not a direct function of winding currents, but it's proportional to the volt-seconds λ_1 applied to the winding (3.55). In a typical high frequency design the peak-peak flux density swing is large and limited by the core loss, not by the saturation level. Usually both core and copper loss have to be taken into consideration.

$$\Delta B = \frac{\lambda_1}{n_1 \cdot A_c} \quad (3.55)$$

More detail about losses in other magnetic components one can find in [47].

3.6 Capacitor

In many cases a capacitor is treated as a lossless component. In fact it's not lossless. The complete equivalent circuit of a real capacitor is presented on Figure 3.14 a). It contains the ideal capacitor C , the parallel resistance R_p , the series resistance R_s and the stray inductance L_s . If the capacitor operates well below it's resonance frequency then the stray inductance L_s is neglected and the complete equivalent circuit reduces. Figure 3.14 b) presents the series equivalent circuit, which contains the ideal capacitor C and so called equivalent series resistance ESR. From the power loss point of view ESR is the key component and the capacitor power loss is given by (3.56) in a general case. ESR value is sometimes available in the capacitor datasheet.

$$P_C = \text{ESR} \cdot I_{C(\text{rms})}^2 \quad (3.56)$$

However many manufacturers publish so called dissipation factor (or loss factor) $\tan\delta$ instead of ESR. The dissipation factor is given by (3.57) and relates to the parallel equivalent circuit presented on Figure 3.14 c). The circuit contains the ideal capacitor C and the parallel resistance R_p , which originally represented the finite resistance of the capacitor dielectric material. Unfortunately the parallel circuit is not convenient for the analysis, since the capacitor current $i_C(t)$ splits into two currents flowing thru the capacitor C and the parallel resistor R_p . Using (3.58) and (3.59) one can find ESR based on the dissipation factor $\tan\delta$ and transform the parallel circuit into the series circuit. The capacitance C remains not affected.

$$\tan \delta = \frac{1}{2 \cdot \pi \cdot f \cdot C \cdot R_p} \quad (3.57)$$

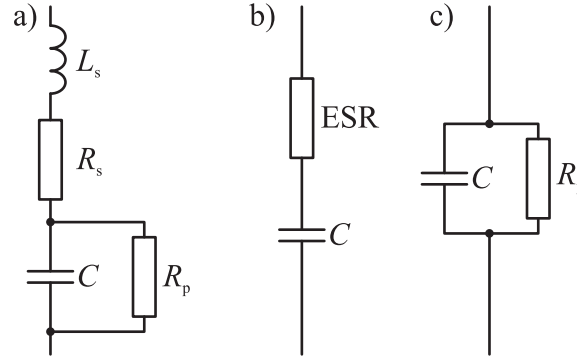


Figure 3.14 Capacitor equivalent circuits - a) complete; b) series; c) parallel

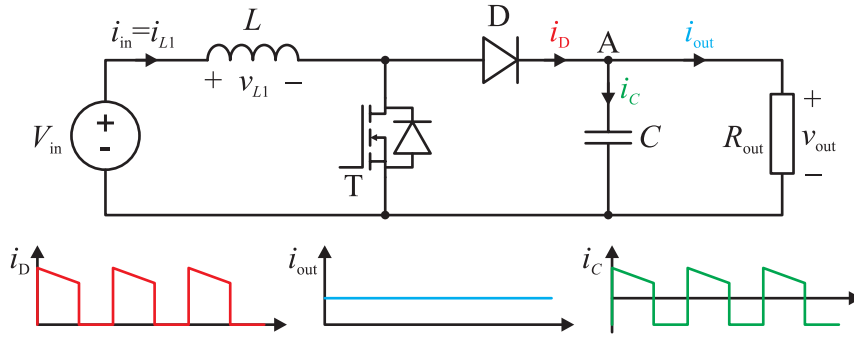


Figure 3.15 Current flow in a boost converter's node A

$$R_p = \frac{1}{2 \cdot \pi \cdot f \cdot C \cdot \tan \delta} \quad (3.58)$$

$$\text{ESR} = \text{Re} \left(\frac{R_p \cdot \frac{1}{(j \cdot 2 \cdot \pi \cdot f \cdot C)}}{R_p + \frac{1}{(j \cdot 2 \cdot \pi \cdot f \cdot C)}} \right) \quad (3.59)$$

Analysis of the series equivalent circuit is fairly easy since there is only one path for the capacitor current $i_C(t)$. To find the capacitor current $i_C(t)$ let's consider the node A of the boost converter presented on Figure 3.15. The diode D conducts unidirectional pulse width modulated current, which contains ac and dc components. Assuming that the output capacitor C is large and the output voltage ripple is negligible, the output current is pure dc current I_{out} . So, the ac component of the diode current can flow only thru the capacitor C . Moreover, it's well known that in steady state there is no dc current in any capacitor. So, the rms capacitor current is given by (3.60). In many cases it's enough to estimate the power loss in the capacitor, but for some types of capacitors ESR (or $\tan \delta$) is a strong function of the frequency. In such case it's possible to use harmonic analysis of the capacitor current and find the power loss caused for each harmonic.

$$I_{C(\text{rms})} = \sqrt{I_{D(\text{rms})}^2 - I_{\text{out}}^2} \quad (3.60)$$

3.7 Other losses

Losses described in sections from 3.3 to 3.6 above are associated with particular components in the power circuit of the converter and they are major part of total losses inside the converter. In a low power converters (let's say below 100 W) losses coming from the control circuitry (analog, microcontroller, DSP or similar) and from the measurement circuitry and sensors may become a significant part of total losses. In medium / high power converters (let's say above 1000 W) these losses are usually fairly small in compare to the power circuit losses.

Any commercial converter has to fulfill certain requirements regarding harmonics and EMI pollution [73, 74]. It means that the converter has to be equipped with input and output filters or EMI filters. Such filters are built from passive components (magnetics and capacitors), so they suffer the same kind of losses like passive components in the power circuit.

In a low voltage / high current application a substantial conduction loss may occur in a high current path (PCB track or busbar) and interconnections. So, in such case it's necessary to ensure a large enough copper cross section area. Moreover, one shall be aware of the skin effect in case of an ac current path. Such an ac wiring should be as short as possible too in order to reduce a stray inductance and improve EMI performance. More details and guidelines about a layout design one can find in [75].

For the power loss estimation purposes none of these losses is taken into account. It simplifies calculations on the one hand. On the other hand gives a good basis for a fair comparison between different topologies.

3.8 Model verification

The modeling approach and models presented in Chapter 3 have to be verified and 200 W boost converter is built for this purpose. All kinds of losses discussed in previous paragraphs exist in this simple topology, so they can be calculated, measured and verified. Verification process is done in following steps:

- validation of the converter model
- components parameters extraction
- calculation of losses
- measurement of losses

First, the averaged model of the boost converter is compared against the circuit simulator based model. The focus is on current values crucial for the power loss estimation. It includes: the input current, the transistor rms current, the diode current, the output current and currents values just before and just after switching. Results of the comparison are summarized in Table 3.1. A good agreement confirms usefulness of the presented modeling approach.

Table 3.1 Currents calculated by the PLECS model and the averaged model

	PLECS	Averaged model
Input dc current [A]	4.51	4.50
Input peak-peak current [A]	7.70	7.69
Transistor rms current [A]	4.10	4.10
Transistor turn-on / turn-off currents [A]	0.64 / 8.35	0.65 / 8.35
Diode rms current [A]	2.91	2.90
Output dc current [A]	1.50	1.50

Table 3.2 Operating points used for the model verification

	Reference	1	2	3	4
Input voltage [V]	30	<u>20</u>	30	30	30
Output voltage [V]	90				
Output power [W]	135	135	<u>200</u>	135	135
Gate resistor [Ω]	18	18	18	<u>5</u>	18
Inductor (low / high core loss)	low	low	low	low	<u>high</u>

Next, components parameters are extracted and losses are calculated. Most of required parameters are read from components' datasheets and only very few are extracted from measurements (e.g. inductor winding resistance). Power losses are calculated for the reference operating point first. Then, a single operational parameter is disturbed in this way, that only a single kind of loss varies significantly, while other remain about the same. Tested operating points are presented in Table 3.2 while calculated power losses are summarized in Table 3.3.

Finally, power losses in the breadboard are measured. The total converter loss is found with used of precise multimeters, as a difference between the input power and the output power (3.61). This measurement is usually enough to justify efficiency of a breadboard. Unfortunately data collected in this way are insufficient for the model verification. Knowledge about loss distribution in the converter is a must. In an ideal case each kind of loss in each component shall be known. In practice it's easy to find some kind of losses (e.g. conduction losses), while a direct measurement of some others is hard (e.g. the switching loss or the core loss).

$$P_{\text{loss}} = P_{\text{in}} - P_{\text{out}} \quad (3.61)$$

The inductor copper loss is fairly easy to find, since it's easy to measure the inductor current – the dc component $I_{L\text{dc}}$ is measured with a precise ampmeter while the peak-peak value $i_{L(\text{pp})}$ is measured with a current probe. The inductor dc and ac resistances are measured with a high precision RLC-meter.

Estimation of the transistor conduction loss bases on the on-state resistance read from the datasheet and the measured transistor rms current. A direct measurement of the current is difficult, because it's a high frequency current path and use of a

precise ampmeter is not possible, while accuracy of current probes is insufficient. However, the transistor rms current may be calculated from the inductor current and the duty cycle (3.62). Now, the transistor conduction loss is found too.

$$I_{T(\text{rms})} = I_L \cdot \sqrt{1 + \frac{1}{3} \cdot \left(\frac{\Delta i_L}{I_L} \right)^2} \cdot \sqrt{D} \quad (3.62)$$

A direct measurement of the transistor switching losses is straightforward in the theory, but in practice it is not easy. It requires a very fast high voltage probe and a special current sensor, which can be placed directly on the transistor lead (e.g. Rogowski coil). Next, the time delays of the voltage sensing path and the current sensing path have to match exactly. In case of a very fast transistor switching a limited bandwidth may lead to a significant measurement error. Here, a method based on the transistor temperature measurement is proposed. First, the transistor is placed on a separate heatsink and the turned-on transistor is connected to a dc voltage source. The transistor drain current, the drain-source voltage drop and the temperature are measured, so the relation between the transistor loss and the temperature are found. This method has an additional benefit of measuring the actual on-state resistance of the transistor, so datasheet values are verified too. Then the transistor with the heatsink are placed in the converter. During normal operation of the boost converter the following losses dissipate in it: the transistor conduction loss, the transistor switching loss, the diode reverse recovery loss and the loss related to the diode capacitance. Since the transistor conduction loss is known, the remaining part relates to the switching loss.

The diode losses are estimated in the same way like the transistor loss was. First, the diode is placed on a separate heatsink and the heatsink temperature versus conduction loss is measured in dc conditions. Then, the diode together with the heatsink are placed in the converter, so the temperature of the heatsink indicates the total diode loss.

The capacitor loss due to ESR may be found by a direct measurement of the capacitor current $i_C(t)$. In many cases however the capacitor leads are very short and it's not possible to connect any current sensor or ampmeter. In such a case analysis of the diode current and the output current is useful, like described in section 3.6. ESR of the capacitor may be read from the datasheet, but for better accuracy it's measured with a precise RLC-meter.

Now the only remaining loss in the power circuit of the boost converter is the inductor core loss. Measurement of the core loss usually bases on observation of the hysteresis loop [70, 76]. This method requires however an additional equipment, like a hysteresis loop tracer. In the breadboard two inductors are used. The first is designed in the way that the flux density amplitude is very small and the core loss is very small too. The other inductor is designed to have a significantly higher flux density amplitude, so the core loss become a visible part of the total converter loss. Both inductors have a similar inductance value, so the input current waveform shall not be affected, thus other losses remain about the same. The core loss is considered as a remaining part of the converter total losses according to (3.63).

Table 3.3 Power loss simulation (calculation) results

	Reference	1	2	3	4
Transistor conduction loss	0.29	0.74	0.64	0.29	0.29
Transistor switching loss	0.62	0.82	0.85	0.25	0.62
Diode conduction loss	0.93	1.01	1.49	0.93	0.93
Core loss	0.24	0.13	0.24	0.24	1.73
Ac copper loss	0.41	0.25	0.42	0.41	0.14
Dc copper loss	0.11	0.24	0.23	0.10	0.05
Capacitor loss	0.03	0.04	0.06	0.03	0.03
Total calculated loss	2.63	3.23	3.93	2.25	3.79

Table 3.4 Power loss measurement results

	Reference	1	2	3	4
Transistor total loss	0.94	1.56	1.57	0.55	0.94
Diode total loss	0.99	1.16	1.62	0.97	1.01
Estimated core loss	0.26	0.15	0.26	0.26	1.87
Ac copper loss	0.41	0.25	0.41	0.41	0.14
Dc copper loss	0.11	0.24	0.24	0.10	0.05
Capacitor loss	0.03	0.04	0.06	0.03	0.03
Measured total loss	2.74	3.40	4.16	2.32	4.04

$$P_{Fe} = P_{loss} - (P_{Tcond} + P_{Tsw}) - P_{Dcond} - P_{Trr} - P_{Cuac} - P_{Cude} - P_C \quad (3.63)$$

The converter losses are measured in several operating points, like it was simulated before. Table 3.3 and Table 3.4 contain results of simulations and measurements.

Chapter 4

Design and Optimization of the Converter

The converter comparison made in Chapter 2 clearly indicated the non-isolated push-pull-boost converter as a good candidate for a fuel cell converter. In this chapter design and optimization of this topology is presented. It starts with a detailed analysis of the converter, with a special focus on magnetic components operating under different conditions. Then a preliminary calculations are done and power semiconductors are selected among available state-of-the-art components. The last part of this chapter deals with optimization of magnetic components. It's presented that integration of the inductor and the push-pull transformer leads to a significant size reduction compared with the push-pull-boost converter with separated inductor and the transformer.

4.1 Converter analysis

In this section the non-isolated push-pull-boost converter, presented on Figure 4.1, is discussed. For reader convenience the basic operating stages, already presented in paragraph 2.2.6, are described again. Then more detailed discussion of the converter operation is provided in following paragraphs.

This topology originally was presented in [44] and it's called the boost converter based on three-state switching cell by the authors. In [31] a detailed description of the converter, together with key equations and waveforms, is provided. It makes a

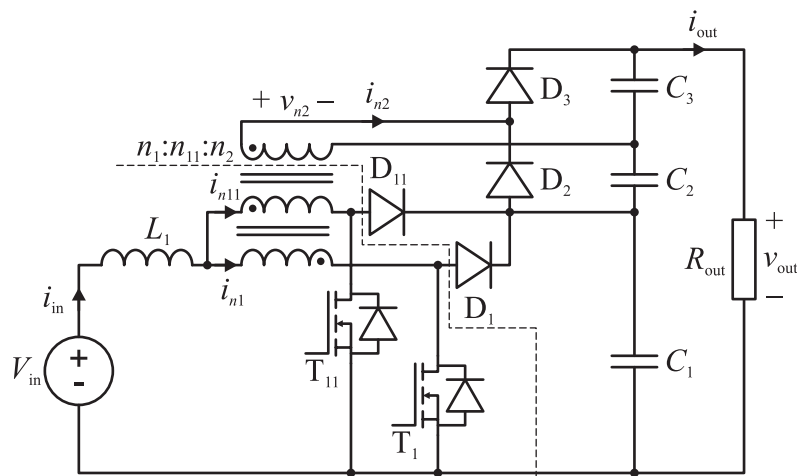


Figure 4.1 The non-isolated push-pull-boost converter diagram

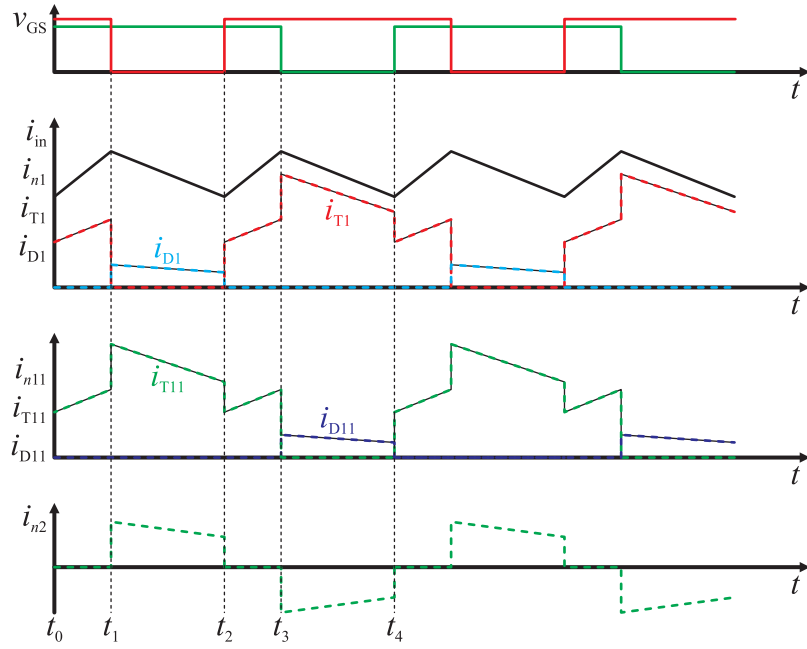


Figure 4.2 Key waveforms of the converter operating in overlapping mode

base for the converter analysis presented in following text.

The converter may be split into two parts, like it's shown by the dashed line on Figure 4.1. The high current part of the converter consists of the inductor, primary windings of the push-pull transformer and both transistors. The low current part consists of all diodes, the secondary side of the transformer and capacitors. Basically the converter operates in CCM with the duty cycle above 50% (conditions for operation with the duty cycle below 50% are introduced in section 4.1.2). Gate signals are 180° phase shifted, like presented on Figure 4.2. Under this conditions in a steady state the converter has four operating stages. Two of them (1 and 3) are identical, while two remaining stages (2 and 4) are symmetrical.

Stage 1 lasts from time t_0 to t_1 . During this stage both transistors are turned-on and diodes D_1 and D_{11} are reverse biased. Primary windings of the transformer are shorted and the primary voltage is zero during this period. So, the secondary voltage is zero too and diodes D_2 and D_3 are reverse biased. The load is supplied from the output capacitors during this period. Neglecting the primary winding resistance and the transistor on-state resistance the whole input voltage V_{in} is applied to the inductor L_1 . The inductor current ripple amplitude is given by (4.1). By rearranging (4.1) the inductance L_1 is found with (4.2).

$$\Delta i_{L1} = \frac{V_{in} \cdot (D - 0.5)}{2 \cdot L_1 \cdot f_s} \quad (4.1)$$

$$L_1 = \frac{V_{in} \cdot (D - 0.5)}{2 \cdot \Delta i_{L1} \cdot f_s} \quad (4.2)$$

Stage 2 lasts from t_1 to t_2 . At the beginning of this stage the transistor T_1 is turned-off and it remains off until time t_2 . Because there is a non-zero leakage

inductance of the winding (not shown on Figure 4.1) the current $i_{n1}(t)$ is commutated from the transistor T_1 to the diode D_1 . The diode is forward biased now, so the capacitor voltage $v_{C1}(t)$ is applied to series connected primary windings. A positive voltage $v_{n2}(t)$ induces in the secondary winding and if the induced voltage is higher than the capacitor voltage ($v_{n2}(t) > v_{C3}(t)$), then the diode D_3 become forward biased. Energy stored in the inductor L_1 during stage 1 is now transferred to output capacitors C_1 and C_3 .

Stage 3 lasts from t_2 to t_3 and it's identical to stage 1. Stage 4 lasts from t_3 to t_4 and it's symmetrical to stage 2, while the transistor T_{11} is turned-off. During stage 4 capacitors C_1 and C_2 are recharged.

4.1.1 Voltage gain

The static voltage gain of the converter is found by analysis of the inductor volt-second balance [47] and assuming that capacitor voltages have negligible ripples. From the inductor L_1 point of view there are only two operational stages in CCM – charging periods (stages 1 and 3) and discharging periods (stages 2 and 4). During the charging period the input voltage is applied to the inductor and the volt-second λ_{L1+} is given by (4.3). During the discharge period the voltage across the inductor equals the difference between the input voltage and the half of the capacitor voltage V_{C1} , since $n_1 = n_{11}$. The volt-second λ_{L1-} applied to the inductor during this period is given by (4.4). Now, both volt-seconds during charging and discharging periods have to stay in balance. Now, equations (4.3) and (4.4) are combined in such a way that they describe the capacitor voltage V_{C1} (4.5). Capacitor voltages V_{C2} and V_{C3} are found with (4.6). The output voltage V_{out} is a sum of capacitor voltages given by (4.7), so the voltage gain is given by (4.8).

$$\lambda_{L1+} = \frac{V_{in}}{f_s} \cdot (D - 0.5) \quad (4.3)$$

$$\lambda_{L1-} = \frac{\left(\frac{V_{C1}}{2} - V_{in} \right)}{f_s} \cdot (1 - D) \quad (4.4)$$

$$V_{C1} = V_{in} \frac{1}{1 - D} \quad (4.5)$$

$$V_{C2} = V_{C3} = \frac{n}{2} \cdot V_{C1} \quad (4.6)$$

$$V_{out} = V_{C1} + V_{C2} + V_{C3} = \frac{n+1}{1-D} \cdot V_{in} \quad (4.7)$$

$$M = \frac{V_{out}}{V_{in}} = \frac{1+n}{1-D} \quad (4.8)$$

4.1.2 Duty cycle below 50%

An isolated current-fed push-pull converter cannot operate with duty cycle below 50% in CCM. It's simply because a continuous current path for the inductor current has to be ensured, so at least one of transistors has to be turned-on. The non-isolated version of this converter overcomes this limitation. Diodes D_1 and D_{11} provide a continuous path for the inductor current, when both transistors are off.

Before converter's operation with the duty cycle below 50% is discussed let's take a look on what happen at 50% duty cycle. In this operating point there are only two operating stages – 2 and 4, when one transistor is turned-on and the other is turned-off. Stages 1 and 3 don't exist since there is no overlapping here. There are no inductor charging or discharging periods, the input current is ideally smooth and the inductor voltage $v_{L1}(t)$ is zero all the time. The input voltage V_{in} is applied directly to one of primary windings and since $n_1=n_{11}$ the capacitor voltage V_{C1} has to be twice the input voltage (4.9). The output voltage is given by (4.10). If the duty cycle $D=50\%$ is substituted into (4.7) one can see that (4.7) and (4.10) equals each other – so the voltage gain is continuous on this boundary.

$$\frac{V_{C1}}{V_{in}} = \frac{n_1 + n_{11}}{n_1} = 2 \quad (4.9)$$

$$V_{out} = 2 \cdot (1 + n) \cdot V_{in} \quad (4.10)$$

Now, the duty cycle decreases below 50% slightly and there are four major operating stages again. Figure 4.4 presents related waveforms. Stages 1 and 3 are symmetrical – one transistor is turned-on and the other is turned-off. Stages 2 and 4 are identical – both transistors are turned-off.

During stage 1 the transistor T_1 is turned-off and the diode D_1 conducts. The capacitor voltage V_{C1} is applied to series connected primary windings of the

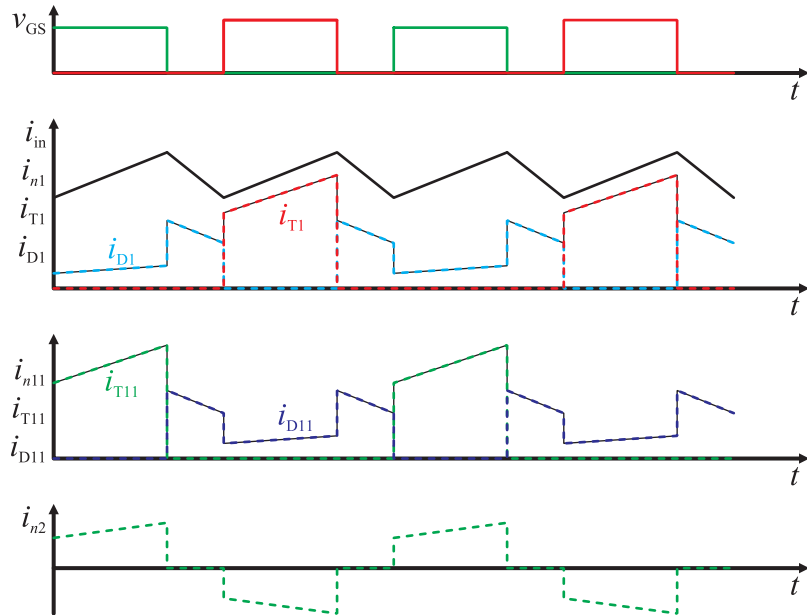


Figure 4.3 The converter waveforms at duty cycle lower than 50%

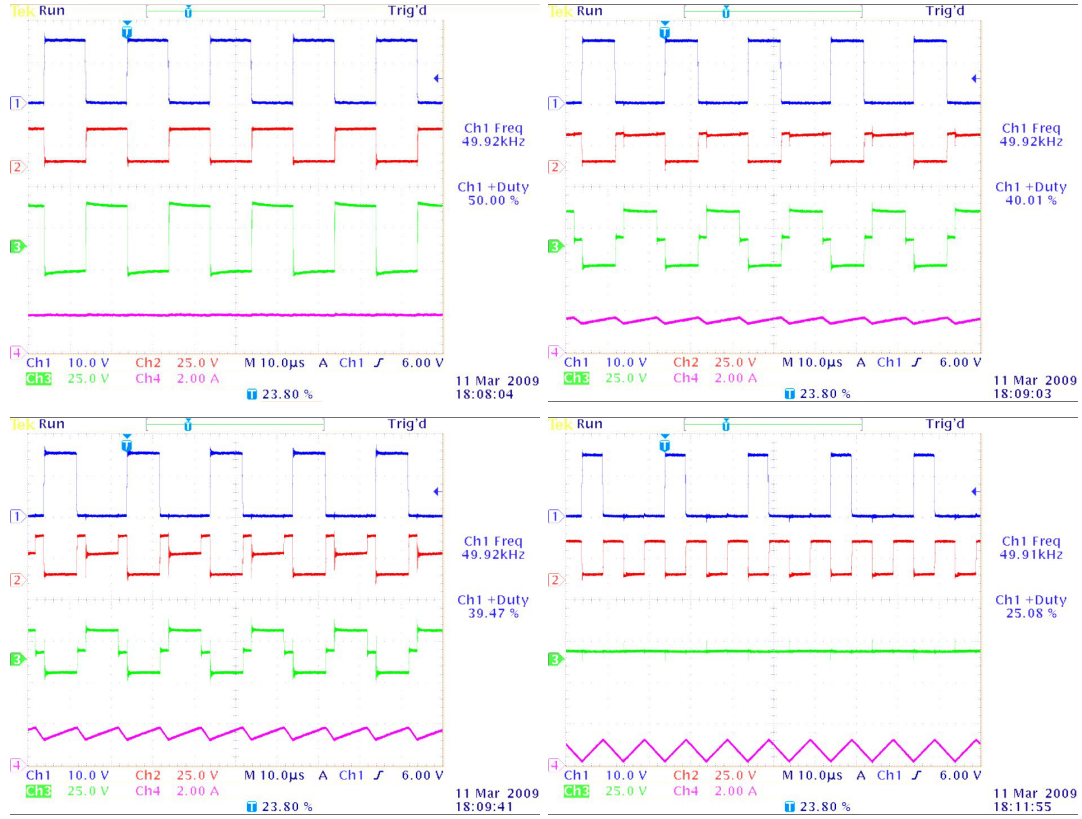


Figure 4.4 The converter observed waveforms while operating with duty cycle of 50% (top-left), 40% (top-right), 39.5% (bottom-left) and 25% (bottom-right), Ch1 – the gating signal for T_1 ; Ch2 – the drain-source voltage of T_1 ; Ch3 – the secondary winding voltage; Ch4 – the inductor current

transformer. Also the positive voltage induces in the secondary winding and the capacitor C_3 is charged thru the diode D_3 .

During stage 2 both transistors are turned-off and diodes D_1 and D_{11} conducts. Primary windings are effectively shorted and there is no voltage across the secondary winding.

Stage 3 is symmetrical to stage 1 and stage 4 is identical to stage 2.

The capacitor voltage V_{C1} is higher than the input voltage V_{in} . Stages 2 and 4 are considered as the inductor discharging periods, while stages 1 and 3 are charging ones. The voltage gain is found by analysis of the inductor volt-second balance and it's given by (4.11).

$$M = \frac{V_{out}}{V_{in}} = \frac{1+n}{1-D} \quad (4.11)$$

However it's found empirically that at lower duty cycles the voltage gain doesn't follow (4.11). Figure 4.4 presents observed waveforms for duty cycles below 50%. It's clear that at one point the secondary voltage (the voltage across capacitors C_2 and C_3) collapses and only the capacitor C_1 contributes to the output voltage. Observed waveforms look like in a two phase boost converter with a coupled inductor (see section 2.2.2). The voltage gain of the converter is measured and

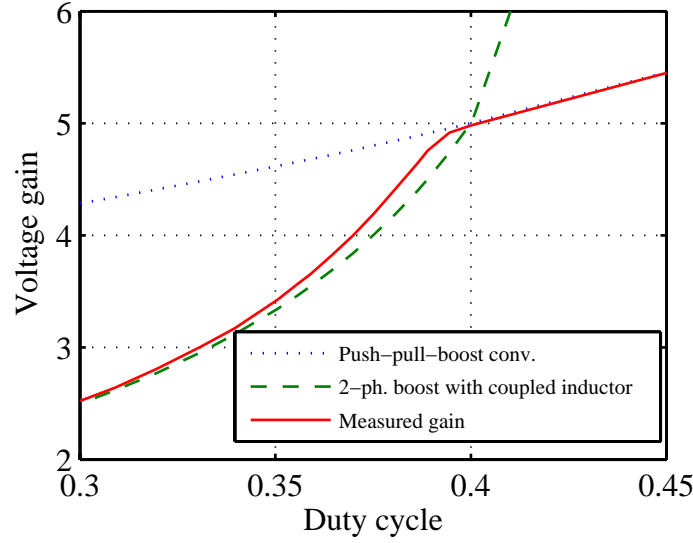


Figure 4.5 Measured voltage gain of the converter vs. theoretical gain given by (2.15) and (4.11)

compared with prediction given by (4.11) for the non-isolated push-pull converter and (2.15) for the two phase boost with the coupled inductor. Figure 4.5 shows the result. Above the crossing point the voltage gain follows (4.11) and below the crossing point it follows (2.15). The critical duty cycle (at the crossing point) is given by (4.12).

$$D_{cr} = \frac{n}{2 \cdot n + 1} \quad (4.12)$$

It's very important to note that the converter may operate safely with duty cycle between 50% and the critical duty cycle. However operation below the critical duty cycle is not recommended since the whole output voltage appears across the capacitor C_1 only. So, both transistors and diodes D_1 , D_{11} may experience an excessive and undesired voltage stress.

4.1.3 Currents

Respective dc, rms and ac currents are calculated using the method briefly introduced in paragraph 3.2.1 and using general equations (4.13), (4.14) and (4.16).

$$I = \sum_{k=1}^n \left(\frac{t_k - t_{k-1}}{t_n - t_0} \right) \cdot \left(\frac{i(t_k) + i(t_{k-1})}{2} \right) \quad (4.13)$$

$$I_{(rms)} = \sqrt{\sum_{k=1}^n \left(\frac{t_k - t_{k-1}}{t_n - t_0} \right) \cdot u_k} \quad (4.14)$$

$$u_k = \frac{1}{3} \cdot \left(i(t_{(k-1)+})^2 + i(t_{(k-1)+}) \cdot i(t_{k-}) + i(t_{k-})^2 \right) \quad (4.15)$$

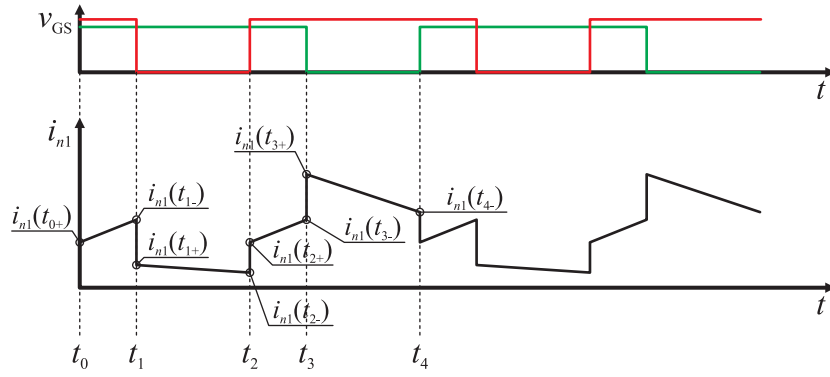


Figure 4.6 The primary winding current waveform and its values at the beginning and at the end of each stage

$$I_{(ac)} = \sqrt{I_{(rms)}^2 + I^2} \quad (4.16)$$

In the non-isolated push-pull-boost converter transistor and diode currents are parts of the primary winding current. To find the primary winding current, and thus the diode and the transistor currents, it's necessary to find the primary current values at the beginning and at the end of each stage (trapezoidal segment), i.e. just before and just after transistor switching, like presented on Figure 4.6. For this purpose following assumptions are made:

- the input current is fairly smooth
- currents $i_{D1}(t)$ and $i_{D11}(t)$ have the same shape like currents $i_{D3}(t)$ and $i_{D2}(t)$ respectively, but they are lower by half (4.17).

$$i_{D1}(t) = \frac{1}{2} \cdot i_{D3}(t) \quad (4.17)$$

During stages 1 and 3 the inductor current splits into two exact halves and flows thru both primary windings. The winding currents are given by (4.18) during these periods.

$$i_{n1}(t_k) = i_{n11}(t_k) = \frac{1}{2} \cdot i_{L1}(t_k) \Big|_{k=0+,1-,2+,3-} \quad (4.18)$$

During stage 2 the winding current $i_{n1}(t)$ flows thru the diode D_1 only. Also the secondary winding current $i_{n2}(t)$ flows thru the diode D_3 only. At any time the sum of the transformer winding currents has to be zero (4.19). Also the inductor current may flow only into primary windings (4.20).

$$i_{n11}(t) - i_{n1}(t) - n \cdot i_{n2}(t) = 0 \quad (4.19)$$

$$i_{L1}(t) = i_{n1}(t) + i_{n11}(t) \quad (4.20)$$

Manipulation of these equations leads to the solution for the winding current $i_{n1}(t)$ during stage 2 (4.21). The other winding current $i_{n11}(t)$ is found with (4.22).

$$i_{n1}(t_k) = \frac{i_{L1}(t_k)}{2 \cdot (1+n)} \Big|_{k=1+,2-} \quad (4.21)$$

$$i_{n11}(t_k) = i_{L1}(t_k) - \frac{i_{L1}(t_k)}{2 \cdot (1+n)} \Big|_{k=1+,2-} \quad (4.22)$$

Stage 4 is symmetrical to stage 2 and primary currents i_{n1} and i_{n11} transpose only ((4.23) and (4.24)).

$$i_{n1}(t_k) = i_{L1}(t_k) - \frac{i_{L1}(t_k)}{2 \cdot (1+n)} \Big|_{k=3+,4-} \quad (4.23)$$

$$i_{n11}(t_k) = \frac{i_{L1}(t_k)}{2 \cdot (1+n)} \Big|_{k=3+,4-} \quad (4.24)$$

Rearrangement of (4.19) results in the equation for the secondary current $i_{n2}(t)$ (4.25) and it's valid for all stages.

$$i_{n2}(t) = \frac{i_{n11}(t) - i_{n1}(t)}{n} \quad (4.25)$$

Now, the inductor current $i_{L1}(t)$ in time instants t_0, t_1, t_2 and so on is found as the minimum or the maximum instantaneous inductor current (4.26). It's assumed that the inductor current is constant during a short switching period – so it's the same just before and just after switching ($i_{in}(t_{k-}) = i_{in}(t_{k+})$).

$$i_{L1}(t_k) = \begin{cases} I_{L1} - \Delta i_{L1} & |_{k=0,2,4} \\ I_{L1} + \Delta i_{L1} & |_{k=1,3} \end{cases} \quad (4.26)$$

In the considered converter respective time instants t_k are found based on the switching frequency f_s and the duty cycle D . Details are presented in Appendix B in form of MATLAB® equations.

4.1.4 Inductor and transformer

The inductor current ripple is proportional to the applied volt-second which is given by (4.27) for the duty cycle above 50%. Figure 4.7 presents the normalized inductor current ripple as a function of the duty cycle. Theoretically, there inductor current is smooth at 50% and 100% duty cycle, while the maximum current ripple occurs at 75% duty cycle. The inductor current contains a large dc component with a limited ac ripple. So, in the inductor design the focus is on a low dc resistance.

$$\lambda_{L1} = \frac{V_{out} \cdot (1-D) \cdot (D-0.5)}{f_s} \quad (4.27)$$

The transformer flux density amplitude ΔB is found by analysis of the volt-second applied to the transformer and it's given by (4.28). The equation is truth for duty cycle above 50%. Figure 4.8 presents the normalized flux density amplitude as a function of duty cycle. The largest flux density exists at 50% duty cycle and it decreases while the duty cycle increases.

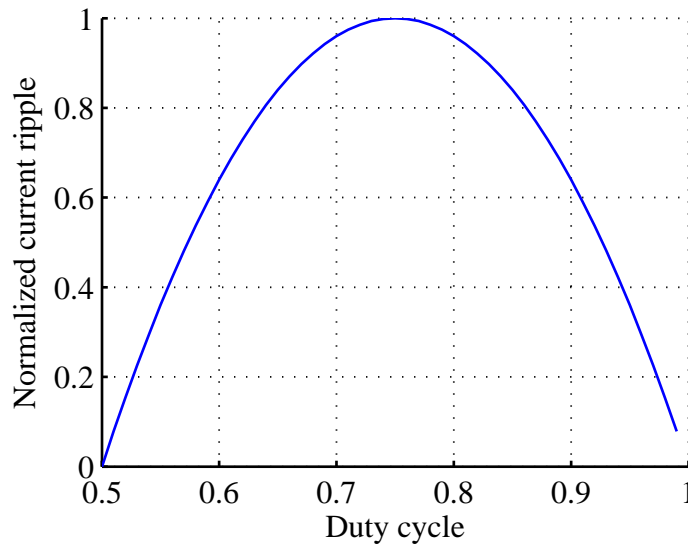


Figure 4.7 The normalized inductor current ripple as a function of the duty cycle

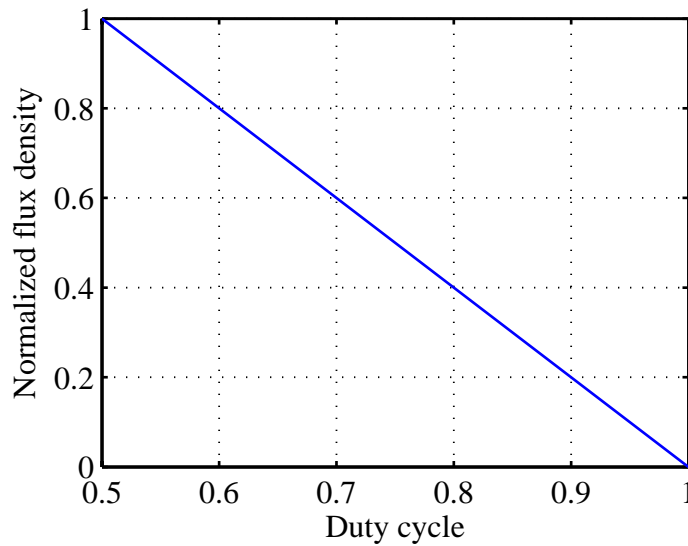


Figure 4.8 The normalized transformer flux density as a function of the duty cycle

$$\lambda_{n1} = \frac{V_{\text{out}} \cdot (1-D)}{f_s \cdot (1+n)} \quad (4.28)$$

At this point it's important to note that each of primary currents contains three components: the half of the input dc current, the half of the input current ac ripple, and the reflected secondary current. All three components are presented on Figure 4.9 and their paths are presented on Figure 4.10. The input current (dc and ac ripple) flows thru the inductor winding and thru primary windings which are effectively in parallel and the resistance seen by this current component is expressed as $R_{L1} + R_{n1} || R_{n11}$. The secondary winding current flows in the secondary winding,

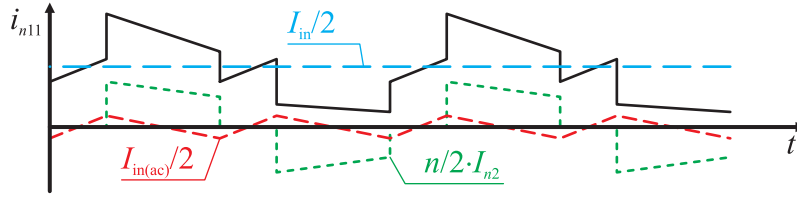


Figure 4.9 The primary current components

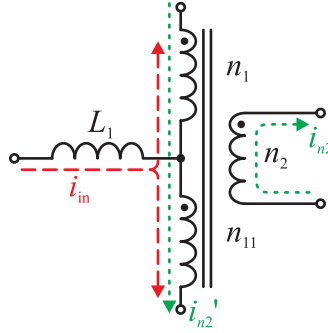


Figure 4.10 Flow of current components in the push-pull transformer

but it's also reflected to the primary windings, which are effectively series connected for this current component and the resistance seen by this current component is expressed as $R_{n2} + R_{n1} + R_{n11}$. So, it's very important to arrange transformer windings in such way, that resistance seen by all current components is low.

4.1.5 Summary

In this section the non-isolated push-pull-boost converter has been analyzed in details. It's operation under different conditions has been explained. Also set of equations describing the converter has been developed and presented to the reader. These equations are included into the averaged converter model, which is used for the converter design process described in following paragraphs.

4.2 Design

In the previous section the non-isolated push-pull-boost converter has been analyzed in details and set of equations have been developed. In this paragraph the preliminary design considerations and calculations are presented.

The specification of the breadboard originate from the project limitations in section 1.4.1 and it's presented in Table 4.1. The primary application is a modular converter for a fuel cell. It results in variable input voltage and gives some freedom in terms of the converter's output power (modularity). So, some provisions are done. The converter's power losses are optimized for the lowest input voltage, which results in the highest input current. However all components have to sustain the highest input voltage. The peak efficiency of 98% leaves a room for only 2% of losses. So, the projected power loss distribution at about half of the rated output power (efficiency peak point) is as follow:

Table 4.1 The specification of the breadboard

Input voltage range $V_{in(min)}-V_{in(max)}$	30-60 V
Output voltage V_{out}	400 V
Rated output power P_{out}	100-1000 W
Input current ripple at rated current $I_{in(pp)}$	20%
Output voltage ripple $V_{out(pp)}$	5%
Target efficiency η	98%

- 0.5% for MOSFETs
- 0.5% for diodes
- 0.5% for the transformer
- 0.3% for the inductor
- 0.2% for capacitors and other losses.

The first step is to find circuit parameters like the turns ratio, the duty cycle range. As mentioned before the converter may operate below 50% duty cycle, but in order to avoid an excessive voltage stress it's desired to operate in overlapping mode and the minimum duty cycle is assumed to be 50%. The maximum allowed turns ratio is found with (4.29) at maximum input voltage $V_{in(max)}$. However use of a foil winding in the transformer requires an integer turns ration, thus $n=2$ is used (see section 4.2.4). The minimum and maximum duty cycle is found at the highest and at the lowest input voltage ((4.30) and (4.31)).

$$n = \frac{V_{out}}{V_{in(max)}} \cdot (1 - D_{(min)}) - 1 = \frac{400}{60} \cdot (1 - 0.5) - 1 = 2.33 \approx 2 \quad (4.29)$$

$$D_{(min)} = 1 - (1 + n) \cdot \frac{V_{in(max)}}{V_{out}} = 1 - (1 + 2) \cdot \frac{60}{400} = 0.55 \quad (4.30)$$

$$D_{(max)} = 1 - (1 + n) \cdot \frac{V_{in(min)}}{V_{out}} = 1 - (1 + 2) \cdot \frac{30}{400} = 0.78 \quad (4.31)$$

At this point two key parameters are still not known – the rated output power and the switching frequency. How to fix them in this case? One can pick the output power and the switching frequency arbitrary and then try to find suitable components – especially transistors. The other way is exactly opposite – find a state-of-the-art transistor first and then find the optimum operating point for it. The second way is shortly described in paragraph 4.2.1. Once the output power and the switching frequency are known, one may calculate currents in the circuit and design magnetic components.

4.2.1 Power MOSFETs

Selection of the most suitable MOSFET is a very important step in any converter design and the choice shall be careful. There are many available MOSFETs, so

Table 4.2 Basic data of IFRP4321PbF MOSFET

Breakdown voltage	150 V
Rated current	78 A
On-state resistance (at 25 °C)	12 mΩ
Total gate charge	71 nC
Input capacitance	4460 pF

how to find the one? How to make sure, that the chosen MOSFET will perform well in the converter?

The first step is very general and simply rejects all parts with inappropriate voltage and current ratings. Only devices which have the current and the voltage rating inside a certain range goes thru to the next step.

The second step bases on so called figure of merit (FOM). In this method the performance of transistor is evaluated based on product of two transistor's parameters. It's important that each of these parameters is directly linked with one of two major loss mechanisms in the transistor – the conduction loss and the switching loss. The most common parameters used are the on-state resistance vs. the total gate charge (4.32) or the on-state resistance vs. the effective output capacitance of the transistor (4.33). It's expected that the device with the minimum FOM will provide the best overall performance, while it minimizes total losses. In fact, the method points out two or three components which are evaluated in the third stage.

$$\text{FOM}_{Q_G} = R_{DS(on)} \cdot Q_{Gtot} \quad (4.32)$$

$$\text{FOM}_{C_{oss}} = R_{DS(on)} \cdot C_{oss} \quad (4.33)$$

Once the transistor is selected the optimum operating point is found. The

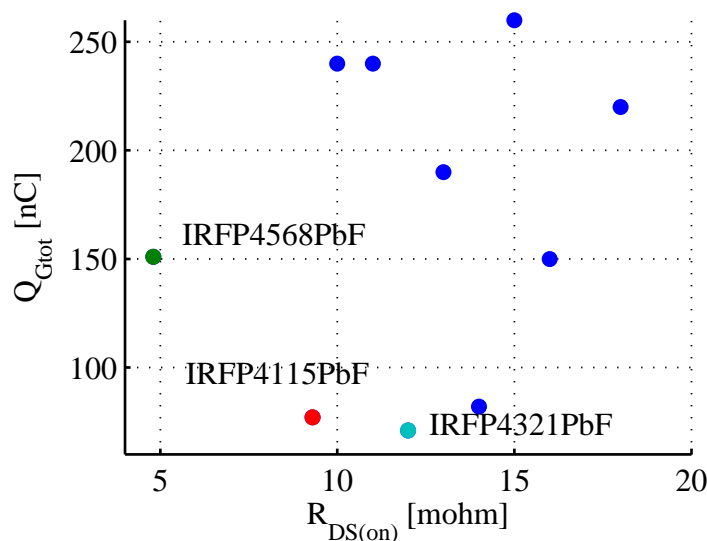


Figure 4.11 On-state resistance vs. total gate charge of several 150 V MOSFETs

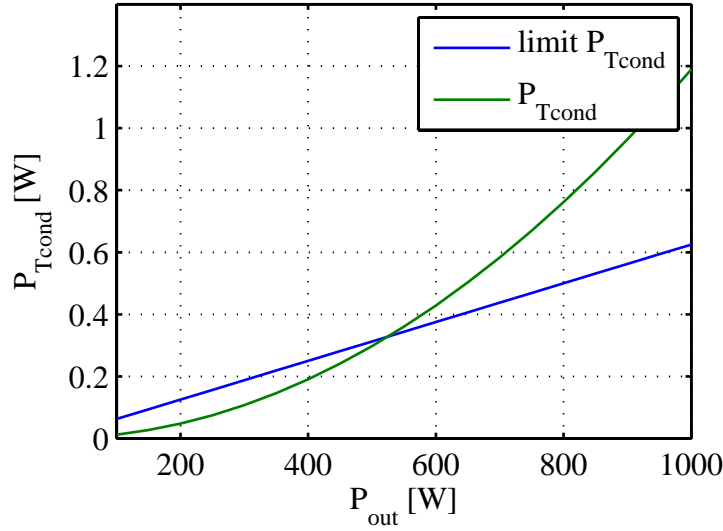


Figure 4.12 The conduction loss limit and the actual conduction loss vs. the output rated power of the converter

averaged converter model and the transistor model (both introduced in Chapter 3) are used to calculate actual power losses in the transistor operating under different conditions.

Now, the numerical example it provided. The wanted transistor is the 150 V rated MOSFET (4.34). After looking at the high power end (1000 W) the transistor's rms current is about 18.1 A (according to (2.62) and the method presented in section 4.1.3). Including the current derating factor between 2-10, the wanted transistor's rated current is between 36.2-181 A. Using a search engine [77] 54 different MOSFETs are found. They are sorted by the on-state resistance and top 10 components go to the second stage. Figure 4.11 shows the on-state resistance vs. the total gate charge of considered MOSFETs. The top three MOSFETs are marked with different colors. At the time of the converter design only IRFP4321PbF [78] was available and since it was superior in compare with other available devices it's selected for further work. Basic parameters of the MOSFET are summarized in Table 4.2.

$$V_{T1(\text{off})} = V_{T11(\text{off})} = V_{D1(R)} = V_{D11(R)} = \frac{1}{n+1} \cdot V_{\text{out}} = \frac{1}{1+2} \cdot 400 = 133.3 \text{ V} \quad (4.34)$$

Once the transistor is selected the next step is to find the optimum operating point for it. This point shall cover the converter peak efficiency point, thus the transistor loss limit is known. It equals 0.5% of the output power at the peak efficiency point. The transistor operates in its optimum when the conduction loss equals the switching loss, so the allowed conduction loss in a single transistor is 0.125% of the converter output power at the peak efficiency point. Figure 4.12 shows the conduction loss limit for a given rated power and the actual conduction loss calculated by the model. The crossing point indicated the optimum rated power, which in this case is about 500 W. So, the expected conduction loss is about 0.31 W per MOSFET at 250 W output power (efficiency peak point). It's

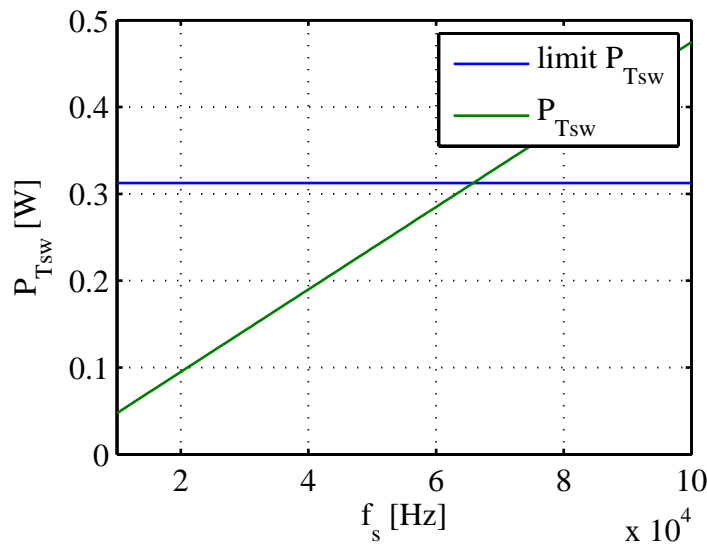


Figure 4.13 The switching loss limit and the actual switching loss vs. switching frequency

important to note that calculations are sensitive to the MOSFET junction temperature, which is 40 °C in this case.

The allowed switching loss is easily found since it equals the conduction loss in the optimum point. Knowledge about the allowed switching loss is used to find the optimum switching frequency. Still, the calculation is not straightforward since the gate drive circuit has a great influence on switching times and the switching loss. For the first approximation the gate circuit parameters are taken from the MOSFET datasheet. Figure 4.13 shows the allowed switching loss and the actual switching loss of the transistor. The crossing point indicated the optimum frequency and it's located close to 65 kHz. In the breadboard the switching loss will increase, because of losses associated with the stray inductance and the diode. So, the switching loss is reduced on account of these additional losses and it's fixed at 50 kHz. In future it's possible to work with the gate drive circuit and optimize switching of the MOSFET.

Now the output rated power and the switching frequency are fixed and they equal 500 W and 50 kHz respectively.

4.2.2 Power diodes

According to the assumed power distribution the allowed total diode loss is 1.25 W at the lowest input voltage and 250 W output power (efficiency peak point). A power diode usually is preselected based on its maximum reverse voltage and forward current values (average, rms and peak) [79]. The choice of the optimum device bases on the forward characteristic (conduction loss) and the switching performance (reverse recovery and junction capacitance).

The reverse recovery loss is recognized as a severe loss mechanism in hard switching converters. This issue is addressed first and the focus is on Schottky diodes only, since they exhibit almost no reverse recovery loss. Moreover,

Table 4.3 Basic data of 30CPQ150PbF Schottky diode

Breakdown voltage	150 V
Rated average current (per leg, at 25 °C)	15 A
Non-repetitive peak current (5 μs sine)	1000 A
Forward voltage drop (at 25 °C, estimated)	0.5 V
Forward resistance (per leg, at 25 °C, estimated)	29 mΩ

Table 4.4 Basic data of IDT10S60C SiC Schottky diode

Breakdown voltage	600 V
Rated average current (at 25 °C)	10 A
Non-repetitive peak current (10 μs)	350 A
Forward voltage drop (at 25 °C, estimated)	0.9 V
Forward resistance (at 25 °C, estimated)	59 mΩ

Schottky diodes have a lower forward voltage in compare with silicon pn-junction diodes having the same breakdown voltage. The price for it would be: a larger reverse leakage current, a larger diode capacitance and a low maximum breakdown voltage (up to 150-200 V) [43], than silicon pn-junction diodes. Since diodes D_1 and D_{11} are 150 V rated (4.35) they are selected among available Schottky diodes. Based on the average forward current requirement (4.29) there are 43 different diodes preselected [77]. Even in spite of the increased diode capacitance the conduction loss is expected to be the dominant loss mechanism. Thus, the diode selection bases on its forward characteristic only and the device with the lowest forward voltage drop is selected – it's 30CPQ150PbF [78] dual in pack diode and the basic parameters are summarized in Table 4.3.

$$V_{D2(R)} = V_{D3(R)} = \frac{1}{n+1} \cdot V_{out} = \frac{1}{1+2} \cdot 400 = 133.3 \text{ V} \quad (4.35)$$

For the given turns ratio diodes D_2 and D_3 require at least 350 V reverse voltage (4.36). There are many 400 V ultra fast silicon diodes available, however their reverse recovery behavior will cause significant losses since the reverse recovery current flows thru several components, like presented on Figure 4.14. Next choice is to use a novel silicon-carbide (SiC) diode instead. Currently SiC diodes are available in 300 V, 600 V and 1200 V classes [80]. Use of a 600 V rated diodes seems to be a safe choice and they are available from few manufacturers. Again, the diodes are preselected based on its average forward current rating. Many devices have a very similar forward voltage drop, however analysis of the forward characteristic clearly indicated that the device with a higher current rating shall provide a lower conduction loss. The diode IDT10S60C [80] is selected and it's basic parameters are summarized in Table 4.4.

$$V_{D2(R)} = V_{D3(R)} = \frac{n}{n+1} \cdot V_{out} = \frac{2}{1+2} \cdot 400 = 266.7 \text{ V} \quad (4.36)$$

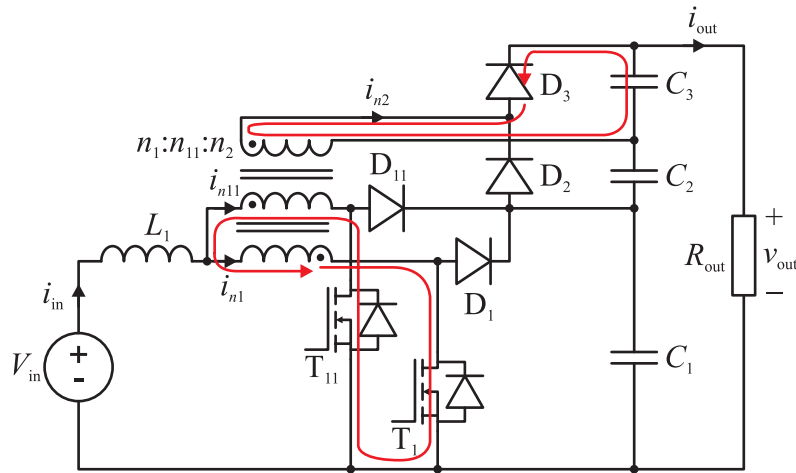


Figure 4.14 The diode D_3 reverse recovery current path

The estimated conduction loss in 150 V diodes is 0.16 W per diode, and in 600 V SiC diodes it's 0.72 W per diode. According to components datasheets there is no reverse recovery loss. The estimated capacitive diode loss in 150 V diodes and 600 V diodes is 0.05 W and 0.07 W per diode. The total estimated power loss in all diodes is about 2 W which exceeds allowed diode loss of 1.25 W. Selected diodes are current state-of-the-art devices and paralleling of them will not reduce the power loss. The only way to keep losses within limits is to reduce losses in other components, like the inductor or the transformer.

4.2.3 Magnetic components

Magnetic components are a very special parts of any power converter. It's because they are designed and optimized for a particular converter, while semiconductors and capacitors are selected among several off-the-shelf parts. Number of available and appropriate parts is limited, so it's relatively easy to find the most suitable one. The choice may base on the component parameters, price or availability. Of course one can find some off-the-shelf inductors or transformers. In many cases these parts may satisfy some of the requirements, but it's most likely that they will not fulfill all of them. The only way is to design and optimize magnetic components specially for the particular converter.

The first step is to choose a core shape and a suitable material. Core manufacturers usually provide core selection guidelines and application notes, where recommendations and practical clues are given. References [41, 81] provide a very good discussion on properties of particular core shapes in different applications. Based on them it's found that EE shaped core is a good candidate to work with. It provides a low winding cost, a simple assembly and a good flexibility. EE cores are available in many different sizes and they are made out of different materials – both ferrite and powder. Also it's fairly easy to place different kind of wires on a EE core, including a Litz wire, a round or a rectangular wire or a foil.

Once the core shape and material are determined, the magnetic device is about to be designed. In the literature one may find several design procedures – some of

Table 4.5 The transformer design input data

Input voltage range $V_{in(min)}-V_{in(max)}$	30-60 V
Output voltage V_{out}	400 V
Rated output power P_{out}	500 W
Switching frequency f_s	50 kHz
Turns ratio	1:1:2
Primary currents $I_{n1} / I_{n1(ac)} / I_{n1(rms)}$ (at 250 W and 30 V)	4.25 / 1.97 / 4.66 A
Secondary current $I_{n2(ac)}$ (at 250 W and 30 V)	1.91 A
Primary currents $I_{n1} / I_{n1(ac)} / I_{n1(rms)}$ (at 500 W and 30 V)	8.68 / 3.92 / 9.52 A
Secondary current $I_{n2(ac)}$ (at 500 W and 30 V)	3.89 A

them are so called single pass procedures, while some others are iterative [43, 47, 82, 83]. In following paragraphs a detailed description of magnetic components design is presented. A single pass area product AP method [43, 83] is used for a core size approximation. Then the core size and basic winding parameters are specified more precisely. Finally FEMM 4.0.1 software is used to minimize windings resistance.

4.2.4 Transformer design

The transformer design input parameters are summarized in Table 4.6. For the transformer core the power ferrite material type P is used [84]. The goal is to keep power losses in the transformer below the limit stated in section 4.2, i.e. 1.25 W at 250 W output power and the lowest input voltage. First, the flux density amplitude is calculated by rearranging natural Steinmetz equation (4.37). The calculation bases on the allowed core loss which shall not exceed 100-150 mW/cm³ in the worst case (the highest winding current).

$$\Delta B = 0.1 \cdot \left(\frac{P_{Fe}}{k \cdot f_s^\alpha} \right)^{\frac{1}{\beta}} = 0.1 \cdot \left(\frac{100}{0.158 \cdot 50^{1.36}} \right)^{\frac{1}{2.86}} = 0.15 \text{ T} \quad (4.37)$$

An appropriate core size is found using the area product method (4.38). Term P_t in the equation is so called apparent power of the transformer and it's defined as the sum of power handled by all windings [83] and it's given by (4.39). For given input parameters the core size equivalent to E42/21/20 [84, 85] is sufficiently large. It's dimensions are summarized in Table 4.6.

$$AP = \frac{P_t}{k_{Cu} \cdot k_f \cdot \Delta B \cdot J \cdot f_s} = \frac{1260}{0.4 \cdot 4 \cdot 0.1 \cdot 4e6 \cdot 50e3} = 3.94 \text{ cm}^4 \quad (4.38)$$

$$P_t = \sum_k I_{nk(rms)} \cdot V_{nk(rms)} = 1260 \text{ VA} \quad (4.39)$$

Next step is to find number of primary winding turns. Two limitation are taken into account. First, as mentioned before the worst case core loss per volume unit shall not exceed 100-150 mW/cm³ and the related flux density amplitude of about

Table 4.6 Dimensions of EE42/21/20 core

Area product (maximum / effective) AP	5.97 / 4.03 cm ⁴
Core cross section A_c	2.44 cm ²
Window dimensions (maximum)	29.6×8.65 mm
Window dimensions (effective)	25.9×6.68 mm
Core volume	22.7 cm ³

Table 4.7 The primary winding number of turns vs. core loss at 30 V input voltage

Number of turns	Flux density amplitude	Core loss per volume	Total core loss
6	0.100 T	32 mW/cm ³	0.73 W
7	0.086 T	21 mW/cm ³	0.48 W
8	0.075 T	14 mW/cm ³	0.32 W
9	0.067 T	10 mW/cm ³	0.23 W

0.15 T. So, the minimum number of turns required to satisfy this limitation is found with (4.40).

$$\begin{aligned}
 n_1 &= \frac{V_{\text{out}} \cdot (1 - D_{(\min)})}{2 \cdot (1 + n) \cdot f_s \cdot A_c \cdot 2 \cdot \Delta B} = \\
 &= \frac{400 \cdot (1 - 0.78)}{2 \cdot (1 + 2) \cdot 50\text{e}3 \cdot 2.44\text{e-}4 \cdot 2 \cdot 0.15} = 4 \text{ turns}
 \end{aligned} \tag{4.40}$$

The second limitation is the maximum allowed power loss in the transformer. Assuming that the core loss equals the copper loss in the maximum efficiency point it allows only 0.625 W of the total core loss, i.e. the maximum core loss per volume unit is 28 mW/cm³ (at the minimum input voltage of 30 V). For different number of turns in primary winding the flux density amplitude and the core loss are calculated. In the first approximation Steinmetz equation is used. Results are summarized in Table 4.7. It's found that 7, 8 and 9 turns fulfill the allowed core loss limitation. However lower number of turns will benefit in lower winding resistance and thus lower copper losses at high power / low input voltage end. For future calculations number of the primary winding turns is 6.

The actual core loss is corrected using modified Steinmetz equation. First, the lowest input voltage case is analyzed. The flux density amplitude is given by (4.41) and its waveform is presented on Figure 4.15. The equivalent frequency and the resulting core loss are found ((4.42) and (4.43)). In the same way the highest input voltage case is analyzed and the calculated core loss per volume unit is about 150 mW/cm³.

$$\Delta B = \frac{V_{\text{out}} \cdot (1 - D_{(\max)})}{2 \cdot (1 + n) \cdot f_s \cdot A_c \cdot 2 \cdot n_1} = 0.1 \text{ T} \tag{4.41}$$

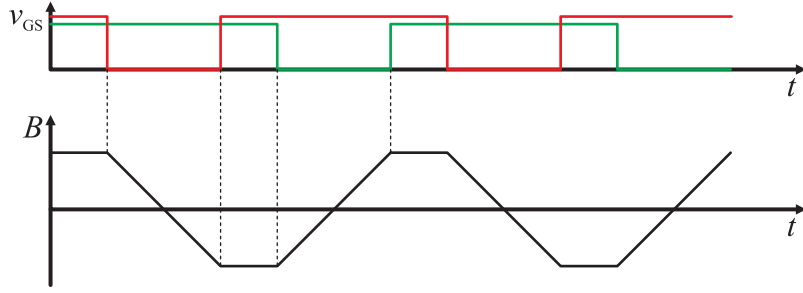


Figure 4.15 The transformer flux density waveform

$$f_{eq} = \frac{2}{\pi^2} \cdot \sum_{k=2}^K \left(\frac{B_k - B_{k-1}}{2 \cdot \Delta B} \right)^2 \cdot \frac{1}{t_k - t_{k-1}} = 90 \text{ kHz} \quad (4.42)$$

$$p_{Fe} = \left(k \cdot f_{eq}^{\alpha-1} \cdot (\Delta B \cdot 10)^\beta \right) \cdot f_r = \quad (4.43)$$

$$= \left(0.158 \cdot 90^{1.36-1} \cdot (0.1 \cdot 10)^{2.86} \right) \cdot 50 = 39 \text{ mW/cm}^3$$

With turns ratio 1:1:2 it gives 12 turns in the secondary winding. For the given rated winding currents (Table 4.5) the minimum cross section areas of winding conductors are found ((4.44) and (4.45)). The minimum window area is calculated with (4.46) and the considered core has the window sufficiently large to accommodate windings.

$$A_{n1} = \frac{I_{n1(rms)}}{J} = \frac{9.52}{4} = 2.38 \text{ mm}^2 \quad (4.44)$$

$$A_{n2} = \frac{I_{n2(rms)}}{J} = \frac{3.89}{4} = 0.97 \text{ mm}^2 \quad (4.45)$$

$$W_{a(min)} = \sum_k \frac{n_k \cdot A_{nk}}{k_{Cu}} = 1.34 \text{ cm}^2 \quad (4.46)$$

The next step is to arrange winding on the core. The primary currents are composed from dc and ac components (see paragraph 4.1.4), which makes the windings design a challenge. Use of a single solid wire may result in a low dc resistance, but because of ac effects (see paragraph 3.5.1) the ac resistance will be large and the ac copper loss may become unacceptably high. In high frequency transformers Litz wires are used to reduce ac resistance and thus related losses. However Litz wires have a poor copper fill factor and the winding dc resistance increase in compare with a solid wire. Keeping a low dc resistance in a push-pull transformer is important too. A foil winding may be a good alternative. It may provide a good copper fill factor (depends on foil and isolation thickness) and the dc resistance is low. Moreover, if the foil winding is built-up from thin layers (in compare with the penetration depth) then the ac loss may stay low. However foil windings may have a significant interwinding capacitance because of a winding large area facing the other winding. To keep this capacitance low an isolation material with a low permittivity. Also a distance between windings is important.

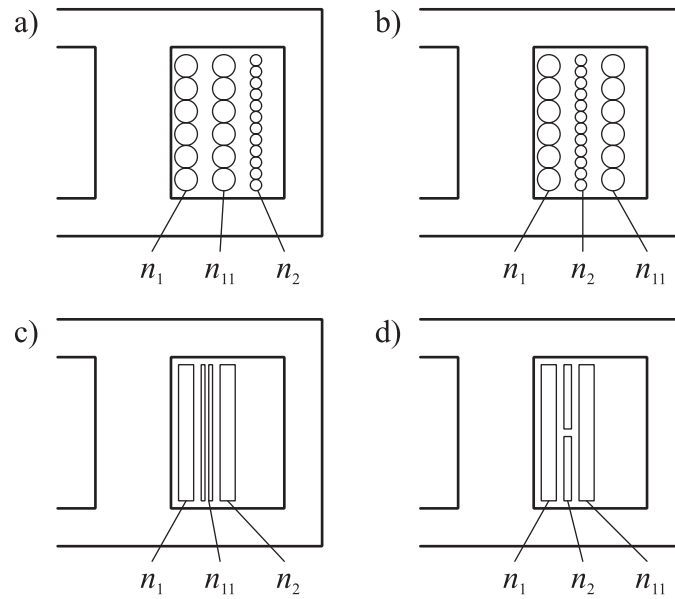


Figure 4.16 Possible winding arrangements of a push-pull transformer on a EE core using solid wires (a and b) and foil (c and d)

Figure 4.16 presents different winding arrangements of a push-pull transformer. The arrangement a) has both primary windings are stacked one on the top of the other. The secondary winding is placed in the top of primary windings. Since the transformer current component sees primary windings as series connected this simple winding arrangement has a large ac loss, because of primary windings multilayer placement. Using interleaving technique the secondary winding may be located between primary windings (Figure 4.16 b). It reduces number of primary winding layers, thus the ac copper loss is reduced. Such a winding arrangement can be implemented using a copper foil. Depends on a layer thickness two solutions for the secondary winding are possible (Figure 4.16 c and d). In both cases the turns ratio is the integer number. The winding arrangement d) has an advantage of less isolation layers in compare with the arrangement c). The winding arrangement d) is used in the design.

The effective window width and height are taken from Table 4.6. The primary winding is made out of 24 mm width foil. To satisfy the required wire cross section area (4.44) the minimum foil thickness is 0.1 mm (0.15 mm is available and used). The secondary winding is made out of 11 mm wide foil and its minimum required thickness is 0.09 mm (0.15 mm is available and used). The transformer operates at 50 kHz and the penetration depth at this frequency is about 0.34 mm. With the layer thickness of 0.15 mm and interleaving a very low ac resistance seen by the transformer current component is expected. Including the isolation of 0.1 mm the total winding height is about 6 mm and it fits the available window size.

Figure 4.17 presents the simulation result of the transformer 2D FEMM model. The current with known amplitude and frequency is applied to windings and copper losses are calculated in each layer. Next, the resistance (dc or ac) is calculated and extrapolated from 2D model to 3D.

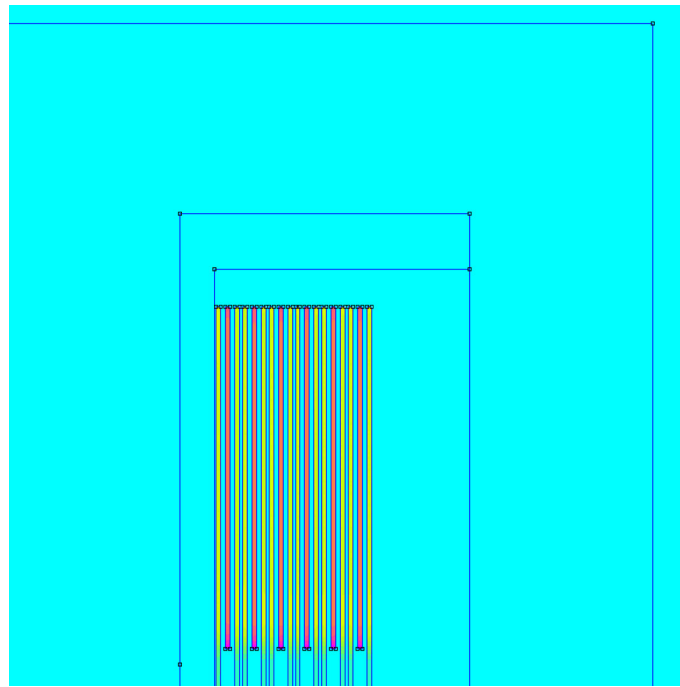


Figure 4.17 The push-pull transformer FEMM model

Table 4.8 The transformer resistances and power losses

Calculated primary winding resistance (dc / ac)	2.7 / 2.9 mΩ
Calculated secondary winding resistance (dc / ac)	11 / 12.5 mΩ
Calculated primary winding copper loss at 250 W (dc / ac)	0.05 / 0.02 W
Calculated secondary winding copper loss at 250 W (ac)	0.05 W
Calculated core loss	0.7W

Table 4.8 summarized the calculated winding resistances and power losses in the transformer operating at the output power of 250 W and the input voltage of 30 V. The estimated winding losses are about 0.21 W and the core loss is about 0.7 W. The total calculated transformer loss is below assumed limit. However, the core loss calculation is valid for the core temperature of 80 °C and since the transformer will operate well below this temperature the actual core loss may increase (according to datasheet plots). Since temperature coefficients ct , ct_1 and ct_2 (see paragraph 3.5.2) are not known the temperature influence is not calculated. Also, since there is window area available it's possible to increase number of turns (e.g. up to 8 primary winding turns) in order to reduce the core loss by the price of a larger winding resistance.

4.2.5 Inductor design

The design input parameters are summarized in Table 4.9. The core material is selected first. For dc inductors powder cores are used often. However they exhibit a non-negligible core loss at higher frequencies, i.e. KoolMu material at 100 kHz and 50 mT has the core loss of about 200 mW/cm³. Ferrite core made out of P

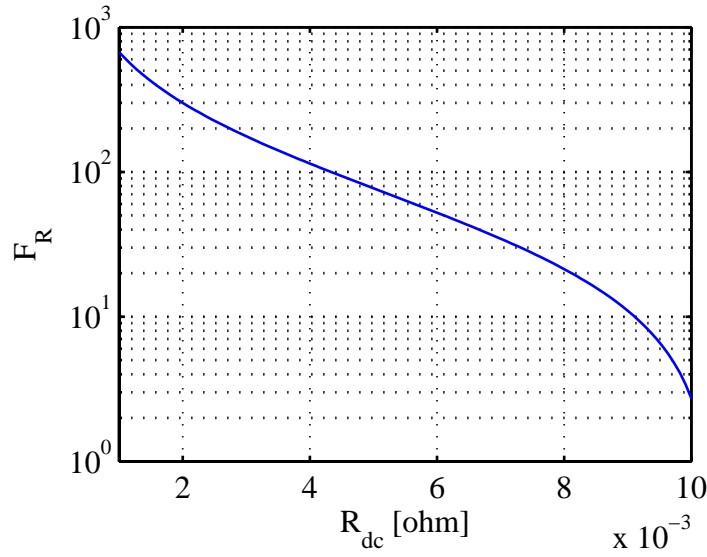


Figure 4.18 Allowed ac to dc resistance factor F_R as a function of the dc resistance of the inductor winding

material [84] is used instead of a powder core. The dissipated power is one of the most important constraints in the design. To reach the efficiency goal the allowed power dissipation in the inductor is about 0.75 W at 250 W output power and the lowest input voltage. To fulfill this requirement both – dc and ac resistance have to stay below the certain limit. Figure 4.18 presents the maximum allowed ac to dc resistance factor F_R as a function of the actual dc resistance of the inductor winding.

The required inductance L_1 is found for the minimum input voltage (i.e. maximum duty cycle) and the rated input current (4.47). The design bases on a gapped ferrite core and it's assumed that the inductor operates in its linear region. So, the flux density is proportional to the inductor current, thus the dc and ac flux density components are found ((4.48) and (4.49)). The area product method links the core dimensions (window area and core cross section area) with the inductor electric and magnetic parameters (like the energy stored in the air gap, the current density or the peak flux density). For given input parameters the required area product is calculated (4.50) and it's found that core size equivalent to E42/21/15 [84, 85] is large enough. It's dimensions and parameters are summarized in Table 4.10.

$$L_1 = \frac{V_{in(min)} \cdot (D_{(max)} - 0.5)}{2 \cdot \Delta i_{L1} \cdot f_s} = \frac{30 \cdot (0.78 - 0.5)}{2 \cdot 1.74 \cdot 50e3} = 48.3 \mu H \quad (4.47)$$

$$B = B_{(max)} \cdot \frac{I_{L1}}{I_{L1(max)}} = 0.35 \cdot \frac{17.4}{19.1} = 0.32 \text{ T} \quad (4.48)$$

$$\Delta B = B_{(max)} - B = 0.35 - 0.32 = 0.03 \text{ T} \quad (4.49)$$

$$AP = \frac{L_1 \cdot I \cdot I_{(max)}}{k_{Cu} \cdot B_{(max)} \cdot J} = \frac{48.3e-6 \cdot 17.4 \cdot 19.1}{0.4 \cdot 0.35 \cdot 4e6} = 2.87 \text{ cm}^4 \quad (4.50)$$

Table 4.9 The inductor design input data

Input voltage range $V_{in(min)}-V_{in(max)}$	30-60 V
Output voltage V_{out}	400 V
Rated output power P_{out}	500 W
Switching frequency f_s	50 kHz
Turns ratio	1:1:2
Input current ripple at rated current $I_{in(pp)}$	20%
Input current I_{L1} (at 250 W and 30 V)	8.5 A
Input currents I_{L1} (at 250 W and 30 V)	17.4 A

Table 4.10 Dimensions of EE42/21/15 core

Area product (maximum / effective) AP	4.74 / 3.17 cm ⁴
Core cross section A_c	1.85 cm ²
Window dimensions (maximum)	29.6×8.65 mm
Window dimensions (effective)	26.2×6.79 mm
Core volume	17.3 cm ³
Center leg dimensions $a \times b$	12.2×15.2 mm

Then the number of turns and the air gap length are found ((4.51) and (4.52)). In the air gap the flux is spread over a larger area, thus the effective air gap area is larger than the core cross section area and it is given by (4.53). Once the effective air gap area is known, the number of turns is corrected (4.54).

$$n = \frac{L_1 \cdot \Delta i_{L1}}{\Delta B \cdot A_g} = \frac{48.3e-6 \cdot 1.74}{0.03 \cdot 1.85e-4} = 15.1 \approx 15 \text{ turns} \quad (4.51)$$

$$l_g = \frac{\mu \cdot n^2 \cdot A_g}{L_1} = \frac{4e-7 \cdot \pi \cdot 15^2 \cdot 1.85e-4}{48.3e-6} = 1.1 \text{ mm} \quad (4.52)$$

$$A_g' = (a + l_g) \cdot (b + l_g) = 2.03 \text{ cm}^2 \quad (4.53)$$

$$n' = \sqrt{\frac{L_1 \cdot I_g}{\mu \cdot A_g'}} = \sqrt{\frac{48.3e-6 \cdot 1.1e-3}{4e-7 \cdot \pi \cdot 2.03e-4}} = 14.4 \approx 14 \text{ turns} \quad (4.54)$$

The number of turns and the length of the air gap are known now. In following steps the minimum wire cross section area is found (4.55) based on the inductor rms current. Then the minimum required window area is calculated (4.56). The selected core provides a significantly larger window area.

$$A_{L1} = \frac{I_{L1(rms)}}{J} = \frac{17.43}{4e6} = 4.36 \text{ mm}^2 \quad (4.55)$$

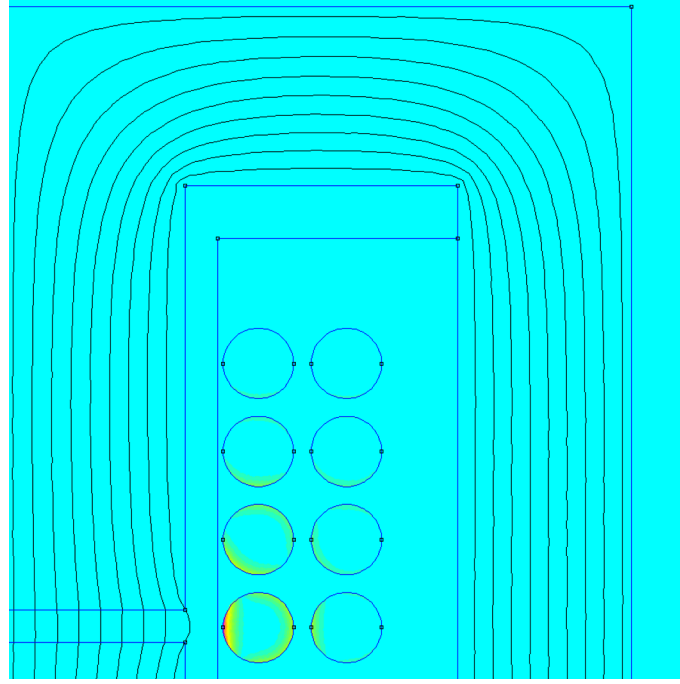


Figure 4.19 FEMM model of the inductor, the winding made out of $\varnothing 2.4\text{mm}$ wire

$$W_{a(\min)} = \frac{n \cdot A_{L1}}{k_{Cu}} = \frac{14 \cdot 4.36\text{e-}6}{0.4} = 1.53 \text{ cm}^2 \quad (4.56)$$

Using modified Steinmetz equation and the method presented in section 3.5.2 the core loss is estimated for the minimum input voltage and the maximum duty cycle. The repetition frequency of the ripple is twice the switching frequency, i.e. 100 kHz. The equivalent frequency is found with (4.57), and it's 82 kHz. The estimated core loss per volume unit is about 0.5 mW/cm^3 (4.58). This calculation doesn't include the core temperature and the dc premagnetization effects, thus the actual core loss may increase. However even if the core loss increases several times of the base value the total core loss will stay low and most likely negligible.

$$f_{eq} = \frac{2}{\pi^2} \cdot \sum_{k=2}^K \left(\frac{B_k - B_{k-1}}{2 \cdot \Delta B} \right)^2 \cdot \frac{1}{t_k - t_{k-1}} = 82 \text{ kHz} \quad (4.57)$$

$$p_{Fe} = \left(k \cdot f_{eq}^{\alpha-1} \cdot (\Delta B \cdot 10)^{\beta} \right) \cdot f_r = \\ = \left(0.158 \cdot 82^{1.36-1} \cdot (0.015 \cdot 10)^{2.86} \right) \cdot 100 \approx 0.5 \text{ mW/cm}^3 \quad (4.58)$$

Now, the winding arrangement is designed. Since the input current has a great dc component and fairly small ac ripple, the focus is on a low dc resistance. The first choice is a solid round wire and the required wire diameter is $\varnothing 2.4 \text{ mm}$. Figure 4.19 presents the winding made out of a single wire arranged into two identical layers. The major drawbacks of this solution includes the difficult winding due to the wire size, partial utilization of the window width, significant ac

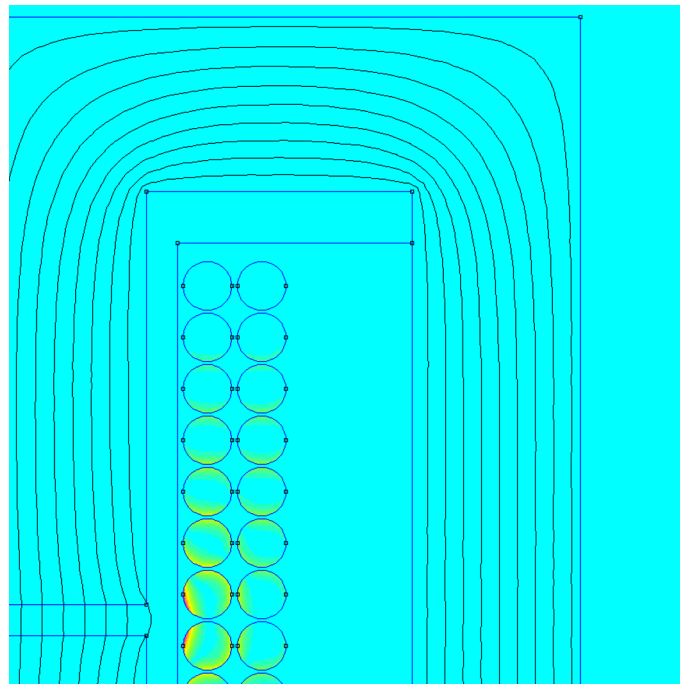


Figure 4.20 FEMM model of the inductor,
the winding made out of two paralleled $\varnothing 1.7\text{mm}$ wires

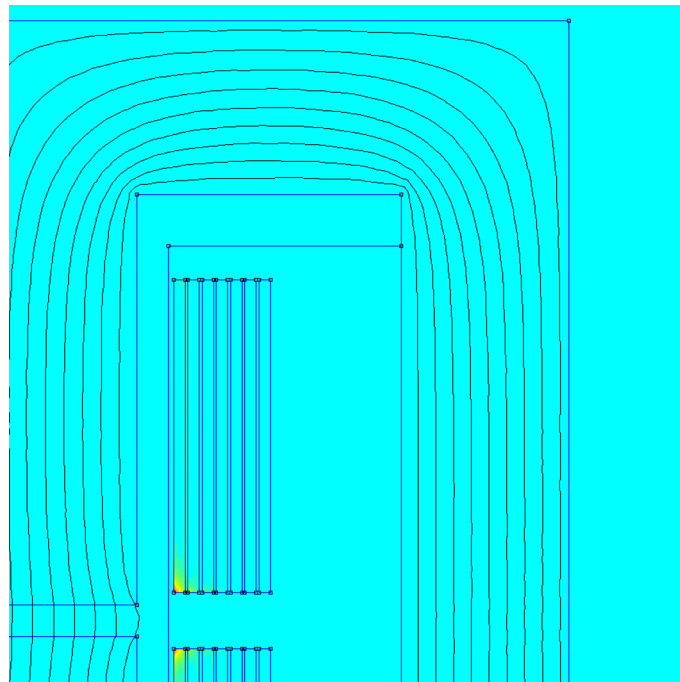


Figure 4.21 FEMM model of the inductor,
the winding made out of $11 \times 0.4\text{ mm}$ foil

loss due to the layer thickness (using Dowell's method the ac to dc resistance factor is about 30).

Use of a several parallel wires, improves the window width utilization and reduces height of the layer in the same time. As a result the ac copper loss may decrease (the ac to dc resistance factor is about 21). Finally, it's easier to wind few

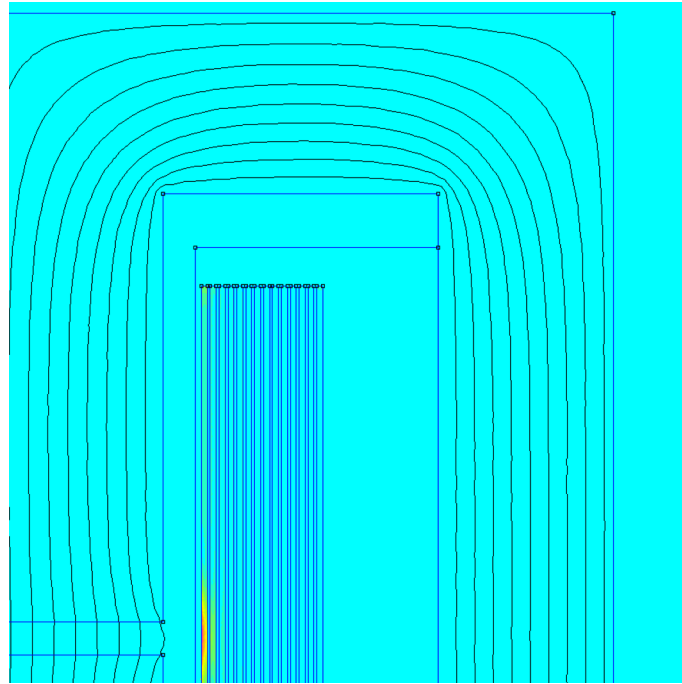


Figure 4.22 FEMM model of the inductor, the winding made out of 24×0.2 mm foil

Table 4.11 Calculated copper losses and winding resistances of the inductor

Wire size / type	Ø2.4 mm	2× Ø1.7mm	11×0.4 mm	24×0.2 mm	24×0.2 mm (notch)
Dc resistance	4.7 mΩ	4.3 mΩ	4.4 mΩ	4.2 mΩ	4.3 mΩ
Ac resistance	0.43 Ω	0.64 Ω	0.3 Ω	0.25 Ω	0.19 Ω
Ac to dc resistance factor	92	149	68	60	44
Dc copper loss (at 250 W)	0.34 W	0.31 W	0.32 W	0.30 W	0.31 W
Dc copper loss (at 500 W)	1.43 W	1.30 W	1.33 W	1.26 W	1.31 W
Ac copper loss (input voltage dependent)	0.43 W	0.65 W	0.30 W	0.25 W	0.19 W

thinner wires than a single thick one. Example of such a winding arrangement using two parallel Ø1.7 mm wires is presented on Figure 4.20.

Add in of parallel wires and reduction of the wire diameter will eventually lead to a foil-like winding, composed of many thin wires placed side by side. Use of a foil winding for a dc inductor may provide a good copper fill factor (depends on a foil wire / isolation thickness ratio) and thus dc copper loss will stay low. Two alternative designs using a foil winding are considered. The first design has 7 layers and 2 turns per layer. Its FEMM model is presented on Figure 4.21. The foil size is 11×0.4 mm and it fits the copper cross section are required by (4.55). Using Dowell's method it's found that the ac to dc resistance factor for this winding configuration is about 37, so the ac loss are relatively high.

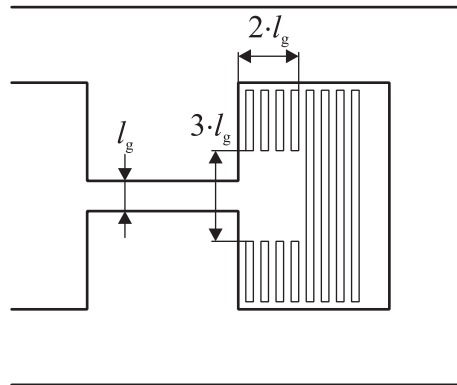


Figure 4.23 Simple rectangular winding notch reducing ac copper loss

The other design has 14 layers, 1 turn per layer and its FEMM model is presented on Figure 4.22. The foil size is 24×0.2 mm and the copper cross section area is larger than required by (4.55). The penetration depth at 100 kHz is about 0.24 mm and the relative penetration depth is 0.8. Using Dowell's method it's found that ac to dc resistance factor F_R for such configuration is about 10.

Dowell's method used for a preliminary estimation of ac copper loss doesn't take into account any effect of an air gap or an edge effect and the ac copper loss may be greatly underestimated. FEMM models (shown on figures above) can predict copper losses accurately and results are summarized in Table 4.11. Both winding arrangements incorporating solid round wire doesn't exceed the allowed loss limit of 0.75 W. The copper loss of foil windings are below the limit and the arrangement presented on Figure 4.22 provides the lowest total copper loss. Further improvement and the loss reduction is possible. Since the winding doesn't occupy whole window it's possible to increase the foil thickness, e.g. up to 0.3 mm and thus reduce the dc copper loss. On Figure 4.22 one may observe a red area in the winding placed close to the air gap. In this part of the winding significant eddy currents are induced by the fringing field around the gap. The method proposed in [56, 61] enables reduction of eddy currents induced by the fringing field simply by removal part of the winding close to the gap. The authors discuss different shapes and sizes of notches and their impact on ac and dc copper losses. However, even a simple, rectangular winding notch presented on Figure 4.23 reduces ac loss by a small cost of increased dc resistance due to a reduced copper cross section area. It's particularly helpful in case of larger air gaps or foil windings placed very close to the gap. In case of the winding from Figure 4.22 the winding is placed on a coil former and it's already relatively distant from the gap. The rectangular notch in fact reduces ac resistance, but in the same time the dc resistance increases. The total copper loss however is reduced by about 10% in compare with a full window width foil winding.

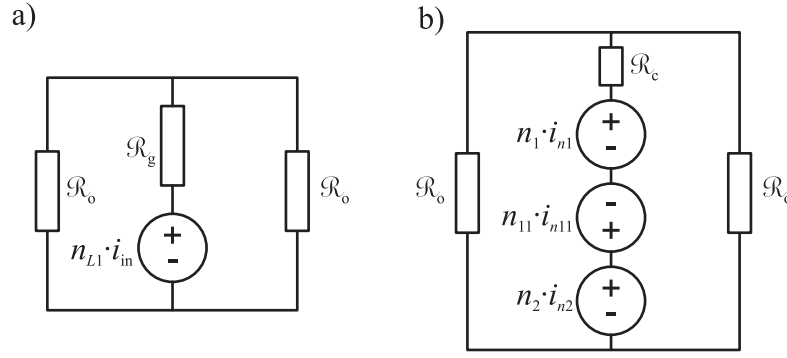


Figure 4.24 Magnetic circuits of gapped inductor (a) and push pull transformer (b)

4.2.6 Integrated inductor-transformer

The concept of integration of the inductor and the transformer on a single core was previously presented in [86] for an isolated Cuk converter and in [87] for an isolated push-pull converter with ripple-free input current.

The input voltage varies in a wide range and the ratio between the minimum and the maximum voltage is 1:2. At the rated power and the lowest input voltage the inductor current reaches its maximum value. The flux density in the inductor core is current dependant and the inductor is designed to sustain the current without core saturation. Contrary to this the flux density amplitude in the transformer core depends on the input voltage and reaches it's maximum at the highest input voltage (and the lowest duty cycle, see Figure 4.8). Moreover, many high frequency transformers are so called thermal limited designs, which means that the maximum flux density amplitude is limited by allowed core loss rather than by saturation level. It leaves some space for dc flux. In this conditions, at the highest input voltage the inductor current may reach about half of the maximum current. So, in terms of flux density only one core at the time is fully utilized, while the other is utilized partially only. The same is true for other current fed dc-dc converters, like full bridge or two inductor boost converter. Moreover, the push-pull boost converter (isolated and non-isolated) suffers an additional copper loss due to the input current flowing thru primary windings. A properly designed integrated inductor-transformer may improve utilization of the magnetic core and windings.

The challenge is to place all windings on a single core in such way that they will not disturb each other, i.e. the ac flux generated by the transformer winding shall not induce any voltage in the inductor winding and vice versa.

Figure 4.24 presents the equivalent circuit of the inductor magnetic circuit. Magneto motive force (MMF) is represented by the voltage source $n_{L1} \cdot i_{L1}(t)$. The reluctance of the center leg including the air gap reluctance is represented by the linear resistor \mathcal{R}_g . Resistor \mathcal{R}_o indicates the outer leg reluctance, but since it's very small in compare with the air gap reluctance it can be neglected.

Figure 4.24 presents the equivalent circuit of the push-pull transformer magnetic circuit arranged on an EE core. All windings are placed on the center leg of the core. MMFs generated by windings are represented by three voltage sources which

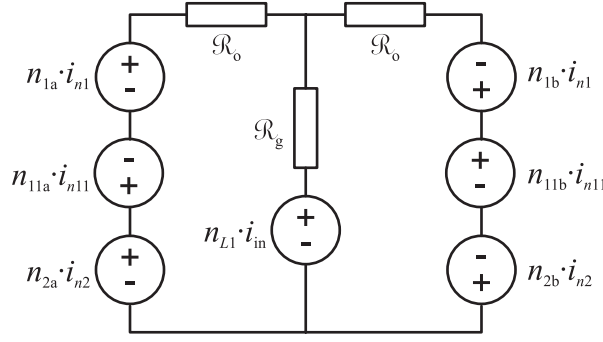


Figure 4.25 Magnetic circuit of integrated inductor-transformer

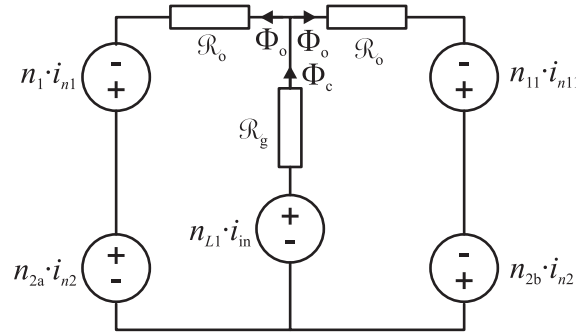


Figure 4.26 Reduced magnetic circuit of integrated inductor-transformer

directions refer to the converter diagram shown on Figure 4.1. Resistors \mathcal{R}_o represent reluctance of outer legs while the resistor \mathcal{R}_c represents reluctance of the center leg without any air gap.

These two magnetic circuits are arranged on a single gapped EE core and Figure 4.25 presents the electrical equivalent circuit. The inductor winding is placed on the center gapped leg. Transformer windings are split into two identical halves and placed on outer legs. In this way there is no undesired interaction between the transformer and the inductor. Fluxes related by the inductor and the transformer are present in outer legs, which in spite of discussion above improves overall utilization of the magnetic core. Unfortunately such winding arrangement is complex. It has a large total number of turns, so copper losses may be high. Another solution is needed.

The inductor current splits into two halves when it flows into transformer primary windings. The flux generated by the inductor winding also splits into two halves once it goes into outer legs. So, there is a good agreement between the inductor current, primary current components and related fluxes and it's possible to use transformer primary windings as a part of the inductor winding. For proper operation of the transformer the secondary winding is split into two symmetrical halves (n_{2a} and n_{2b}) and arranged on both outer legs, so it's not affected by inductor flux. The equivalent circuit of the proposed winding arrangement is presented on Figure 4.26. The proposed integrated inductor-transformer is described by (4.59), where L_k is self inductance of n_k winding, M_{ji} is mutual inductance between n_i and n_j

windings and so on. Self inductances are defined by (4.60) while mutual inductances are given by (4.61) in general case.

$$\begin{bmatrix} v_{L1} \\ v_{n1} \\ v_{n11} \\ v_{n2a} \\ v_{n2b} \end{bmatrix} = \begin{bmatrix} L_1 & M_{L1n1} & M_{L1n11} & -M_{L1n2a} & M_{L1n2b} \\ M_{n1L1} & L_{n1} & -M_{n1n11} & -M_{n1n2a} & -M_{n1n2b} \\ M_{n11L1} & -M_{n11n1} & L_{n11} & M_{n11n2a} & M_{n11n2b} \\ -M_{n2aL1} & -M_{n2an1} & M_{n2an11} & L_{n2a} & M_{n2an2b} \\ M_{n2bL1} & -M_{n2bn1} & M_{n2bn11} & M_{n2bn2a} & L_{n2b} \end{bmatrix} \cdot \begin{bmatrix} \frac{di_{L1}}{dt} \\ \frac{di_{n1}}{dt} \\ \frac{di_{n11}}{dt} \\ \frac{di_{n2}}{dt} \\ \frac{di_{n2}}{dt} \end{bmatrix} \quad (4.59)$$

$$L_k = \frac{n_k^2}{\mathcal{R}_k} \quad (4.60)$$

$$M_{ij} = k_{ij} \frac{n_i \cdot n_j}{\mathcal{R}_{ij}} \quad (4.61)$$

Since outer legs and windings arranged on the core are symmetrical its possible to simplify the matrix in (4.59) because some of mutual inductances are identical (assuming no leakage flux). Reluctance of the center leg, including the air gap, is given by (4.62) and (4.63) gives reluctance of the outer leg. Now respective self and mutual inductances are given by (4.64), (4.65) and (4.66).

$$\mathcal{R}_g = \frac{l_c}{\mu_0 \cdot \mu_r \cdot A_c} + \frac{l_g}{\mu_0 \cdot A_g} \quad (4.62)$$

$$\mathcal{R}_o = \frac{l_o}{\mu_0 \cdot \mu_r \cdot A_o} \quad (4.63)$$

$$\begin{aligned} L_1 &= \frac{n^2}{\mathcal{R}_c + \frac{\mathcal{R}_o}{2}} \\ L_{n1} = L_{n11} &= \frac{n_1^2}{\mathcal{R}_o + \mathcal{R}_g \parallel \mathcal{R}_o} \\ L_{n2a} = L_{n2b} &= \frac{n_{2a}^2}{\mathcal{R}_o + \mathcal{R}_g \parallel \mathcal{R}_o} \end{aligned} \quad (4.64)$$

$$\begin{aligned}
M_{L1n1} &= M_{L1n11} = M_{n1L1} = M_{n11L1} = k_{L1n1} \cdot \frac{n \cdot n_1}{\mathcal{R}_g + \mathcal{R}_o \parallel \mathcal{R}_o} \\
M_{L1n2a} &= M_{L1n2b} = M_{n2aL1} = M_{n2bL1} = k_{L1n2a} \cdot \frac{n \cdot n_{2a}}{\mathcal{R}_g + \mathcal{R}_o \parallel \mathcal{R}_o} \\
M_{n1n11} &= M_{n11n1} = k_{n1n11} \cdot \frac{n_1 \cdot n_{11}}{\mathcal{R}_o + \mathcal{R}_o \parallel \mathcal{R}_g} \\
M_{n1n2a} &= M_{n11n2b} = M_{n2an1} = M_{n2bn11} = k_{n1n2a} \cdot \frac{n_1 \cdot n_{2a}}{\mathcal{R}_o + \mathcal{R}_o \parallel \mathcal{R}_g} \\
M_{n1n2b} &= M_{n11n2a} = M_{n2bn1} = M_{n2an11} = k_{n1n2b} \cdot \frac{n_1 \cdot n_{2b}}{\mathcal{R}_o + \mathcal{R}_o \parallel \mathcal{R}_g} \\
M_{n2an2b} &= M_{n2bn2a} = k_{n2an2b} \cdot \frac{n_{2a} \cdot n_{2b}}{\mathcal{R}_o + \mathcal{R}_o \parallel \mathcal{R}_g}
\end{aligned} \tag{4.65}$$

$$\begin{aligned}
k_{L1n1} &= \frac{\mathcal{R}_o \parallel \mathcal{R}_o}{\mathcal{R}_o} \\
k_{L1n2a} &= \frac{\mathcal{R}_o \parallel \mathcal{R}_o}{\mathcal{R}_o} \\
k_{n1n11} &= \frac{\mathcal{R}_o \parallel \mathcal{R}_g}{\mathcal{R}_o} \\
k_{n1n2a} &\approx 1 \\
k_{n1n2b} &= \frac{\mathcal{R}_o \parallel \mathcal{R}_g}{\mathcal{R}_o} \\
k_{n2an2b} &= \frac{\mathcal{R}_o \parallel \mathcal{R}_g}{\mathcal{R}_o}
\end{aligned} \tag{4.66}$$

Now, so called equivalent inductance L_{1eq} has to be found. During the inductor charging periods (stages 1 and 3, see paragraph 4.1) the input voltage is applied to the inductor winding and parallel connected primary windings of the transformer. In a traditional push-pull transformer primary windings are shorted during this periods and there is no voltage across them (except voltage drop due to wire resistance and leakage inductance), so the whole input voltage is applied to the input inductor. However, in the integrated magnetic device presented on Figure 4.26 primary windings contribute to energy storage and the voltage across them is non-zero. So, (4.67) is truth and L_{1eq} is unknown equivalent inductance. (4.68) and (4.69) are substituted into (4.67). During charging periods there is no current in the secondary winding so (4.70) is truth. Also (4.71) and (4.72) are truth during these periods, so (4.73) gives a solution for the equivalent inductance. It's important to note that the physical inductance of the inductor L_1 may be significantly lower then the equivalent inductance L_{1eq} seen by the converter.

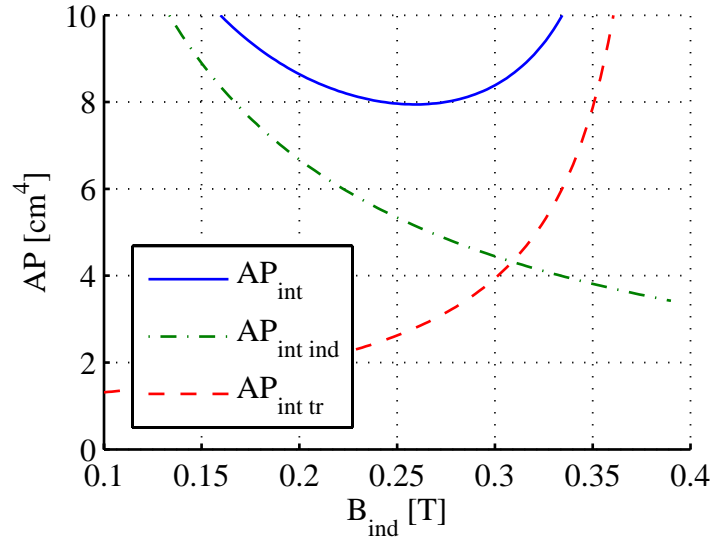


Figure 4.27 Integrated inductor-transformer area product vs. inductor flux density

$$V_{in} = v_{L1} + v_{n1} = L_{leq} \cdot \frac{di_{in}}{dt} \quad (4.67)$$

$$v_{L1} = L_1 \cdot \frac{di_{in}}{dt} + M_{L1n1} \cdot \frac{di_{n1}}{dt} + M_{L1n11} \cdot \frac{di_{n11}}{dt} - M_{L1n2a} \cdot \frac{di_{n2}}{dt} + M_{L1n2b} \cdot \frac{di_{n2}}{dt} \quad (4.68)$$

$$v_{n1} = M_{n1L1} \cdot \frac{di_{in}}{dt} + L_{n1} \cdot \frac{di_{n1}}{dt} - M_{n1n11} \cdot \frac{di_{n11}}{dt} - M_{n1n2a} \cdot \frac{di_{n2}}{dt} - M_{n1n2b} \cdot \frac{di_{n2}}{dt} \quad (4.69)$$

$$\frac{di_{n2}}{dt} = 0 \quad (4.70)$$

$$\frac{di_{n1}}{dt} = \frac{di_{n11}}{dt} \quad (4.71)$$

$$\frac{di_{in}}{dt} = \frac{di_{n1}}{dt} + \frac{di_{n11}}{dt} \quad (4.72)$$

$$L_{leq} = L_1 + M_{L1n1} + M_{n1L1} \quad (4.73)$$

The area product method is used to determine the core size required by the integrated inductor-transformer. For this calculation values from paragraphs 4.2.4 and 4.2.5 are taken. Because two magnetic devices share the same core calculation of the core size is more complex. The simplest way is to add area products required by the transformer and by the inductor (4.74). Since the inductor and the transformer fluxes share the same core the total flux density shall stay below saturation (4.75).

$$AP = \frac{P_t}{k_{Cu} \cdot k_f \cdot \Delta B_{tr} \cdot J \cdot f_s} + \frac{L_1 \cdot I \cdot I_{(max)}}{k_{Cu} \cdot (B_{ind} + \Delta B_{ind}) \cdot J} \quad (4.74)$$

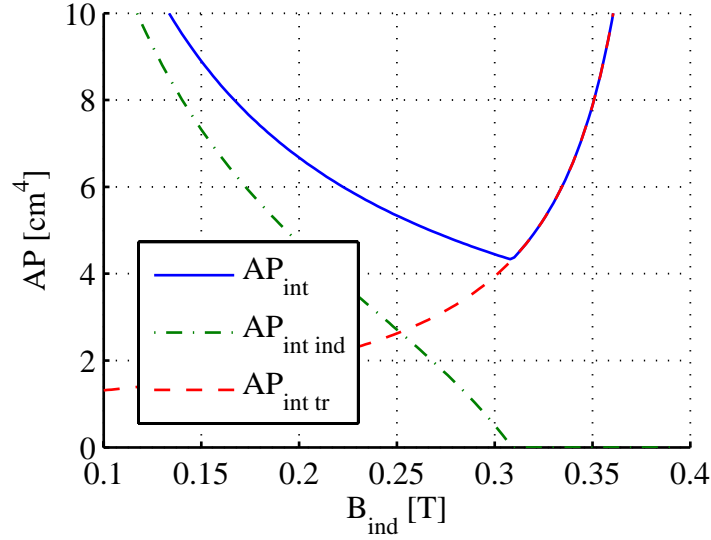


Figure 4.28 Integrated inductor-transformer area product vs. inductor flux density, $B_{\text{sat}}=0.4$ T

$$\Delta B_{\text{tr}} + (B_{\text{ind}} + \Delta B_{\text{ind}}) < B_{\text{sat}} \quad (4.75)$$

By adjusting ratio between the transformer flux density ΔB_{tr} and the inductor flux density ($B_{\text{ind}} + \Delta B_{\text{ind}}$) it's possible to find the minimum required area product of the core, like presented on Figure 4.27. The minimum required area product found in this way equals 7.95 cm^4 and it's significantly larger than the total area product required by separated inductor and transformer (6.80 cm^4). Such a high value is a result of a lower copper fill factor of particular windings and a lower maximum flux density of the inductor.

This simple calculation presented above deals with the transformer and the inductor area products separately and doesn't include some important aspects. Since the transformer flux density amplitude is well below saturation it's possible to inject some significant dc flux without increasing the core size (some additional window area is required however). First the area product required by the transformer only is calculated (4.76). Next, rearrangement of (4.50) enables calculation of how much energy it's possible to store in a given core using only this 'free' flux density space (4.77).

$$AP_{\text{tr}} = \frac{P_{\text{t}}}{k_{\text{Cu}} \cdot k_{\text{f}} \cdot \Delta B_{\text{tr}} \cdot J \cdot f_{\text{s}}} \quad (4.76)$$

$$L_1 \cdot I \cdot I_{(\text{max})} = \frac{AP_{\text{tr}}}{k_{\text{Cu}} \cdot (B_{\text{sat}} - \Delta B_{\text{tr}}) \cdot J} \quad (4.77)$$

The required area product of the core as a function of the inductor flux density is presented on Figure 4.28. For the transformer flux density amplitude below 0.09 T the used core is sufficiently large to handle the inductor. Once the transformer flux density amplitude increases there is not enough 'free' room for the inductor and a bigger core is required. According to this calculation the minimum area product

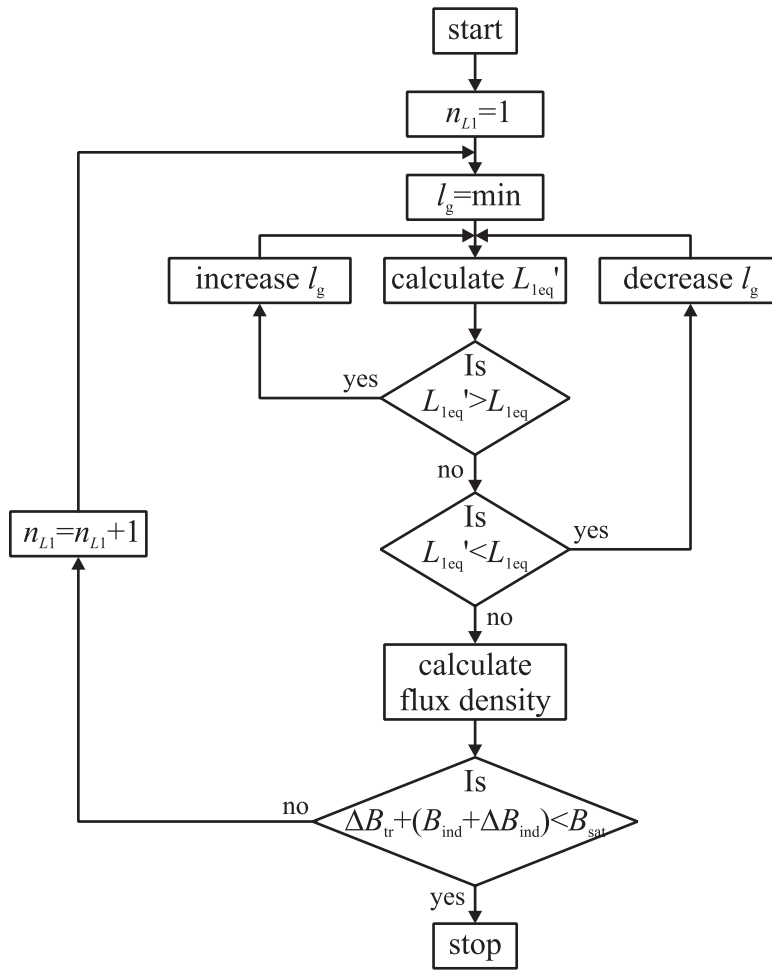


Figure 4.29 The integrated magnetic number of turns and air gap length calculation flowchart

equals 4.33 cm^4 . The core E42/21/20, the one used for the push-pull transformer (see paragraph 4.2.4) is large enough. The optimum inductor flux is about 0.31 T. With assumed saturation level of 0.4 T it leaves about 0.09 T for the maximum amplitude of the transformer flux density. According to calculation from paragraph 4.2.4 the worst case (at the highest input voltage) transformer flux density amplitude is about 0.15 T. However, one shall remember that the dc premagnetization may increase core loss significantly (see paragraph 3.5.2).

Once the core size and core type are known number of turns in particular winding as well the air gap length are calculated. First, the transformer number of turns is found using (4.78). It's important that transformer windings are placed on outer legs, so the effective core cross section area is different from the value given in a standard datasheet.

$$n_1 = \frac{V_{\text{out}} \cdot (1 - D)}{2 \cdot (1 + n) \cdot f_s \cdot A_c \cdot 2 \cdot \Delta B} \quad (4.78)$$

Next, the inductor number of turns and the length of the air gap are calculated in the iterative process, which is shown on Figure 4.29. Starting from a single turn in

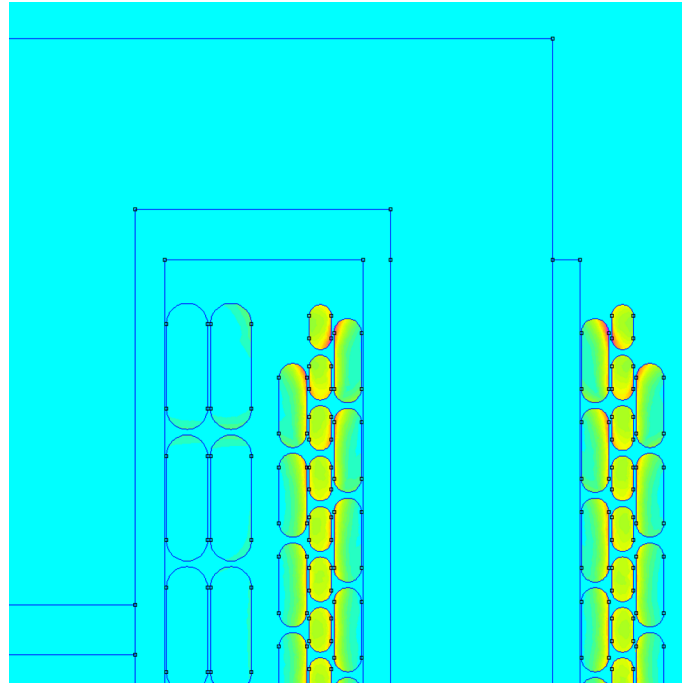


Figure 4.30 FEMM model of the integrated inductor-transformer

the inductor winding the required equivalent inductance is calculated. Successive, ascending air gap length values are substituted into (4.62) and resulting equivalent inductance is calculated with (4.73). This loop is continued until the required equivalent inductance is found. Then the flux densities related to the inductor and the transformer are calculated for different operating conditions. The transformer flux density amplitude is calculated by rearranging (4.78) for a given number of turns. The inductor related flux is found by analysis of the equivalent circuit from Figure 4.26 and it's given by (4.79). From this one can find flux density increase in the center and outer legs due to the inductor.

$$\Phi_c = i_{in} \cdot \frac{n_{L1} + \frac{1}{2} \cdot n_1}{\mathcal{R}_g + \frac{1}{2} \cdot \mathcal{R}_0} \quad (4.79)$$

If the total flux density exceeds the saturation level at any operating point one additional turn is added to the inductor winding and next iteration starts.

Using this method it's found that the transformer primary windings have 13 turns each, the secondary winding has 26 turns (split into two symmetrical halves) and the inductor winding has 10 turns. The air gap length is 1.8 mm. Required wire cross section area doesn't change in compare with previous calculations (4.44), (4.45) and (4.55) that is 4.36 mm² for the inductor winding, 2.38 mm² for the primary winding and 0.97 mm² for the secondary winding. Use of a foil winding become somehow difficult, because of increased number of turns and thus increased interwinding capacitance.

Instead of a foil paralleled round wires are used as follow: inductor winding 3× Ø1.5 mm, primary windings 3× Ø1.0 mm and the secondary winding 2× Ø0.8 mm. The proposed winding arrangement is presented on Figure 4.30.

Table 4.12 The integrated inductor-transformer resistances and losses

Calculated inductor winding resistance (dc / ac ripple)	2.8 / 179 mΩ
Calculated primary winding resistance (dc / ac / ac ripple)	6.9 / 17.2 / 100 mΩ
Calculated secondary winding resistance (dc / ac)	32.7 / 37.5 mΩ
Calculated inductor winding copper loss at 250W (dc / ac ripple)	0.20 / 0.18 W
Calculated primary winding copper loss at 250 W (dc / ac / ac ripple)	0.13 / 0.06 / 0.01 W
Calculated secondary winding copper loss at 250 W (ac)	0.14 W
Calculated core loss	0.29 W

It's important to note that the transformer related flux, the major source of the core loss, flows only in outer legs, so only outer legs contribute to the total core loss. The core loss is calculated using modified Steinmetz equation (see paragraph 3.5.2).

Winding resistances are found using FEMM software and they are summarized in Table 4.12. Also, losses present in the integrated magnetic device are shown in the same table. The total calculated loss of the device operating at 250 W is about 1.2 W. For comparison, the total loss of the push-pull transformer and the dc inductor operating in the same conditions is about 1.14 W.

4.2.7 Capacitors

Output capacitors of the converter are designed to filter high ripples rather than low frequency ripples coming from an inverter. The allowed output voltage peak-to-peak ripple is 5% of the output voltage, i.e. 20 V peak-to-peak. It's assumed that the voltage ripple are distributed among output capacitors according to EQ.

$$\frac{V_{Cj(pp)}}{V_{out(pp)}} = \frac{V_{Cj}}{V_{out}} \Big|_{j=1,2,3} \quad (4.80)$$

According to the converter analysis from paragraph 4.1 the capacitor C_1 is recharged during stages 2 and 4, while it discharges during stages 1 and 3, so effectively it's recharged twice per the switching period. The required capacitance is given by (4.81).

$$C_1 = \frac{I_{out} \cdot (D - 0.5)}{V_{out(pp)} \cdot V_{C1} \cdot f_s} = \frac{1.25 \cdot (0.78 - 0.5)}{5\% \cdot 133.3 \cdot 50e3} = 1.05 \mu F \quad (4.81)$$

The capacitor C_2 is recharged during stage 4 only and discharges during stages 1, 2 and 3. The capacitor C_3 operates symmetrically to the capacitor C_2 and it's charged during stage 2 and it discharges during stages 1, 3 and 4. The required capacitance is given by (4.82).

$$C_2 = C_3 = \frac{I_{out} \cdot D}{V_{out(pp)} \cdot V_{C2} \cdot f_s} = \frac{1.25 \cdot 0.78}{5\% \cdot 133.3 \cdot 50e3} = 2.93 \mu F \quad (4.82)$$

Table 4.13 The loss budget of the 500W converter, output power 250 W, input voltage 30 V

Transistor losses (conduction / switching / gate)	2× 0.32 / 0.32 / 0.07W
Diode losses (low voltage diode / high voltage diode)	2× 0.21 / 0.79W
Transformer losses (copper / core)	0.21 / 0.7 W
Inductor losses (copper dc / ac)	0.31 / 0.19 W
Integrated inductor-transformer (copper inductor / transformer / core)	0.38 / 0.54 / 0.29 W
Other losses (interconnections, capacitors, etc.)	0.5 W
Total loss (with separated / integrated magnetics)	5.11 / 5.13 W

Capacitors are preselected based on their capacitance and their rated dc voltage. Then parts with the lowest ESR are selected – C_1 is 2.2 μF 160 V MKP1839, C_2 and C_3 are 4.7 μF 160 V MKP1839. The capacitor current is found as a difference between the neighboring diode rms current the output dc current. Estimated capacitor loss due to ESR is negligible.

4.3 Summary

In Chapter 4 the non-isolated push-pull-boost converter detailed analysis has been made first and important equations describing the converter has been developed. Next, a numerical example of the converter design has been presented step by step. First, based on the assumed peak efficiency relative loss limits are set. Then, transistors are selected among available state-of-the-art devices and converter parameters (the output power and the switching frequency) are adjusted in the way that transistors are used in optimum way. In following paragraphs other components are selected (diodes, capacitors) or designed (magnetics). The design of the transformer and the inductor bases on a single pass calculations and the area product method for the core size estimation. Winding resistances of a final design are calculated with FEMM software for better accuracy. The final part of the chapter deals with the design of the integrated inductor-transformer for the converter. It's demonstrated that the properly designed integrated magnetic device improves utilization of the magnetic core and winding. As a result the size of magnetic components is significantly reduced, while the calculated losses remains on a comparable level (see Table 4.8, Table 4.11 and Table 4.12).

Finally, the estimated losses of the 500 W converter operating at 250 W output power and 30 V input voltage are summarized in Table 4.13. In both cases (with separated magnetic devices and the integrated one) estimated losses are just about the assumed limit of 5 W. This calculation indicates that the target efficiency is achievable for this converter topology. The calculation however includes only losses in the power circuit of the converter and gate drive loss. It doesn't take into account losses associated with controller and sensor circuitry.

Chapter 5

Modular Converter

A modular converter is not a new concept. This kind of converters are used in telecomm, database and server centers, aerospace and space applications. Modularity provides several well known advantages for both, a system designer and a system user. It includes a system flexibility and scalability, possible cost reduction of installation and maintenance, design standardization and improved reliability due to redundancy. However a simultaneous operation of many converter modules and their interactions creates challenges. The most recognized and pronounced are current/voltage sharing among modules [38, 88-91] and potential system instability due to multiple control loops [92-94].

In this Chapter a general overview on a converter scaling and paralleling is given. Then, different interconnections of converter modules are presented. Finally, benefit of a modular step-up converter in a fuel cell application is demonstrated. It includes a theoretical discussion and practical verification. Also, the idea can be extended for other applications.

5.1 Scaling of converters

The rated output power of a converter is $P_{\text{out(max)}}$ and it's peak efficiency η_{max} occurs at about half of the rated output power $P_{\text{out(max)}}$. The converter is scaled up in power and now the rated power is twice larger $P_{\text{out(max)}}$ '= $2 \cdot P_{\text{out(max)}}$. Efficiency curve shall have the same shape and it peaks at $P_{\text{out(max)}}$ '/2= $P_{\text{out(max)}}$. Since the peak efficiency doesn't change the allowed losses are twice larger now, but the loss distribution shall not change in the scaled converter. How does the scaling process influences particular components?

5.1.1 Transistor

First, transistor losses are considered. At the efficiency peak point the conduction loss equals the switching loss, as explained in paragraph 4.2.1. Once the converter is scaled in power the transistor current and allowed losses increase proportionally (P_{Tcond} '= $2 \cdot P_{\text{Tcond}}$, P_{Tsw} '= $2 \cdot P_{\text{Tsw}}$). Since the conduction loss is proportional to the second power of the current the on-state resistance has to decrease by about half. It's simply done by selection of a larger transistor or by paralleling several devices. Paralleling two or three transistors may be relatively easy, but putting more of them in parallel become a challenge. One of difficulties is to ensure proper layout and equal stray inductances in all current paths. Small

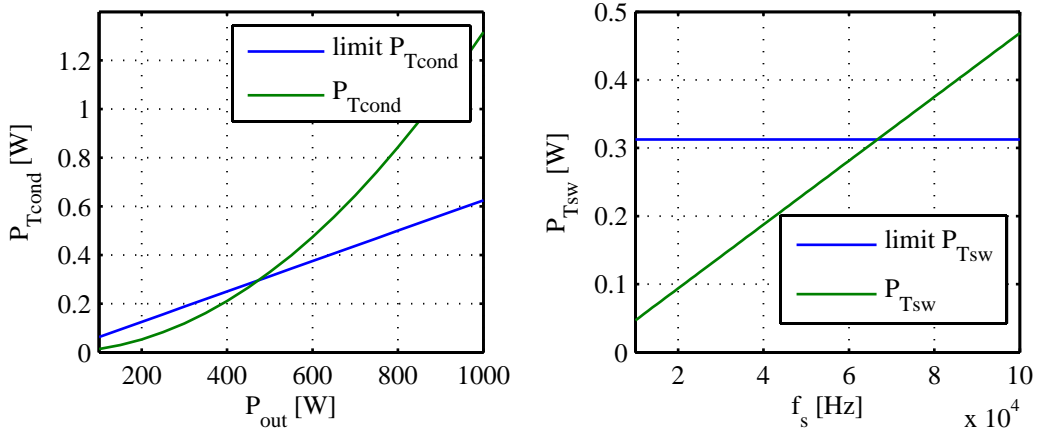


Figure 5.1 Conduction (left) and switching (right) losses of IRFP4321PbF

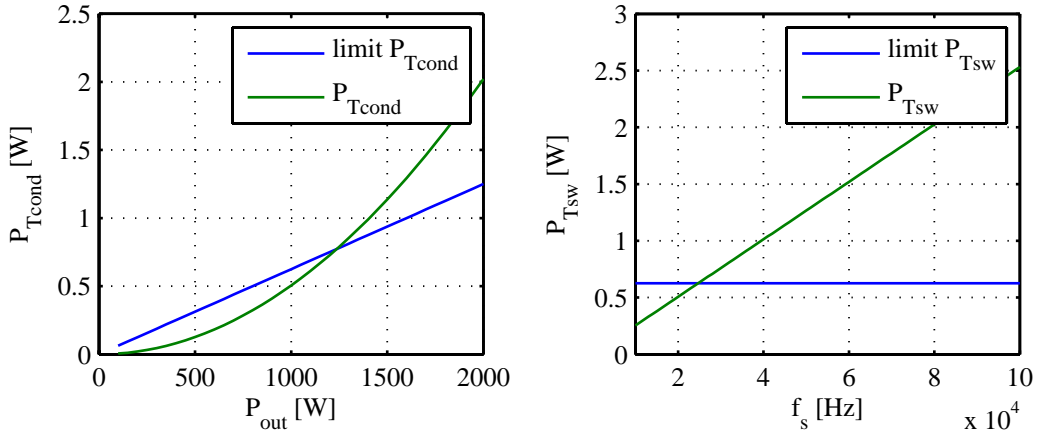


Figure 5.2 Conduction (left) and switching (right) losses of IRFP4568PbF

differences in stray inductances may lead to unexpected voltage oscillations across paralleled MOSFETs [95]. Also dynamic current sharing may become a problem [71]. It may be necessary to reduce switching speed and switching loss may increase. To keep switching loss at acceptable level the switching frequency is reduced. Sometimes however a device having larger current handling capability is available, so there is no need for devices paralleling. Unfortunately in most cases a larger transistor has a worse switching performance.

Here two transistors are compared – IRFP4321PbF and IRFP4568PbF. Both transistors have a similar value of FOM_{QG} but different on-state resistance and switching performance. Results of the comparison are presented on Figure 5.1 and Figure 5.2. In the comparison the current rise/fall rate di_T/dt is assumed to be similar in both cases and it results in different gate resistances. The larger transistor (IRFP4568PbF) is able to process more than twice larger power with the same conduction loss in percentage terms. However keeping the switching loss on the certain level requires a significant reduction of the switching frequency, even in spite a lower gate resistance.

If the converter is being scaled up further it may be necessary to change used technology – it applies to both, layout and transistors. At certain power level it's

use of PCB is not possible anymore, thus busbars are used instead. It potentially results in longer interconnections and it eventually may lead to the switching frequency reduction. In the same time it may be necessary to change transistor technology, e.g. IGBT instead of MOSFET. Certainly such change has an impact on the optimum power level and the optimum switching frequency.

From this point two cases shall be considered – first, the switching frequency of the scaled converter remains the same ($f_s' = f_s$) or second, the switching frequency decreases (for sake of simplicity, by half ($f_s' = f_s/2$)).

5.1.2 Inductor

Now, the boost inductor is being scaled up. Since the allowed current ripple increases the required inductance changes according to (5.1).

$$L_1' = \frac{V_{in(min)} \cdot (D_{(max)} - 0.5)}{2 \cdot \Delta i_{L1}' \cdot f_s'} = \begin{cases} \frac{V_{in(min)} \cdot (D_{(max)} - 0.5)}{2 \cdot 2 \cdot \Delta i_{L1} \cdot f_s} = \frac{1}{2} \cdot L_1 \\ \frac{V_{in(min)} \cdot (D_{(max)} - 0.5)}{2 \cdot 2 \cdot \Delta i_{L1} \cdot \frac{f_s}{2}} = L_1 \end{cases} \quad (5.1)$$

The required core size is found with area product method. Assuming the same maximum flux density, current density and copper fill factor it's given by (5.2).

$$AP' = \frac{L_1' \cdot I' \cdot I_{(max)}'}{k_{Cu} \cdot B_{(max)} \cdot J} = \begin{cases} \frac{\frac{1}{2} L_1 \cdot 2 \cdot I \cdot 2 \cdot I_{(max)}}{k_{Cu} \cdot B_{(max)} \cdot J} = 2 \cdot AP \\ \frac{L_1 \cdot 2 \cdot I \cdot 2 \cdot I_{(max)}}{k_{Cu} \cdot B_{(max)} \cdot J} = 4 \cdot AP \end{cases} \quad (5.2)$$

References [83, 96] provide core dimensions growth guidelines – for linear dimensions (5.3), areas (5.4) and volumes (5.5). So, the core volume will increase by factor of 1.68 if the switching frequency remains constant or by factor of 2.83 if the switching frequency is reduced by half. Moreover it's stated that the current density shall decrease (5.6) because of a relatively smaller increase in the cooling surface.

$$\text{length} = k_{\text{length}} \cdot AP^{\frac{1}{4}} \quad (5.3)$$

$$\text{area} = k_{\text{area}} \cdot AP^{\frac{2}{4}} \quad (5.4)$$

$$\text{volume} = k_{\text{vol}} \cdot AP^{\frac{3}{4}} \quad (5.5)$$

$$J = k_J \cdot AP^{\frac{1}{8}} \quad (5.6)$$

The scaled inductor, similar to the transistor, conducts twice larger current and allowed copper loss is twice larger too. So the dc resistance of the inductor winding, shall decrease by half. When the inductor is being scaled three parameters change – the number of turns n (5.7), the mean length per turn MLT (5.3) and the allowed copper cross section area A_{Cu} . To keep the current density on

the same level the copper cross section area is double and the resulting dc resistance is given by (5.8). In the first case, the dc resistance of the scaled inductor decreases by more than half, so expected dc copper loss increases slower than assumed. In the second case the dc resistance decreases slower then expected, so it may be necessary to increase the wire cross section area and thus reduce the current density. As the result the required area product may increase further due to a lower current density (5.2). Also, in the second case, the total copper area (wire cross section multiplied by number of turns) grows faster then the window area does. It should be take into account too.

$$n' = \frac{L_1' \cdot \Delta i_{L1}'}{\Delta B' \cdot A_g'} = \begin{cases} \frac{\frac{1}{2} L_1 \cdot 2 \cdot \Delta i_{L1}}{\Delta B' \cdot 2^{\frac{3}{4}} \cdot A_g} = 2^{-\frac{1}{2}} \cdot n \\ \frac{L_1 \cdot 2 \cdot \Delta i_{L1}}{\Delta B' \cdot 4^{\frac{3}{4}} \cdot A_g} = 1 \cdot n \end{cases} \quad (5.7)$$

$$R_{dc}' = \frac{n' \cdot \rho \cdot MLT'}{A_{Cu}'} = \begin{cases} \frac{2^{-\frac{1}{2}} \cdot n \cdot \rho \cdot 2^{\frac{1}{4}} \cdot MLT}{2 \cdot A_{Cu}} = \frac{R_{dc}}{2^{\frac{1}{4}}} \\ \frac{n \cdot \rho \cdot 4^{\frac{1}{4}} \cdot MLT}{2 \cdot A_{Cu}} = \frac{R_{dc}}{2^{\frac{1}{2}}} \end{cases} \quad (5.8)$$

Alternatively the required wire cross section area may be estimated for given dc resistance, number of turns and MLT (5.9).

$$A_{Cu}' = \frac{n' \cdot \rho \cdot MLT'}{R_{dc}'} = \begin{cases} \frac{2^{-\frac{1}{2}} \cdot n \cdot \rho \cdot 2^{\frac{1}{4}} \cdot MLT}{\frac{1}{2} \cdot R_{dc}} = 2^{\frac{3}{4}} \cdot A_{Cu} \\ \frac{n \cdot \rho \cdot 4^{\frac{1}{4}} \cdot MLT}{\frac{1}{2} \cdot R_{dc}} = 2^{\frac{3}{2}} \cdot A_{Cu} \end{cases} \quad (5.9)$$

Such increase of the wire size leads to reduction of relative penetration depth ϕ (5.10) and to possible increase of the ac resistance. For a dc inductor conducting a smooth current ac resistance may not be so important, but it has a great impact on performance of a coupled inductor or a flyback transformer. So, for notation simplicity a square wire is considered, but it's valid for round wires as well. In the first case the relative penetration depth increases, thus the skin effect become more painful. On the other hand less turns may result in fewer layers and thus the higher relative penetration depth could be compensated. In the second case reduction of the switching frequency counteract the relative penetration depth which remains constant. With the same number of turns and possibly the same number of layers the ac to dc resistance factor will not change most likely.

$$\phi' = \frac{h'}{\delta'} = \frac{\sqrt{A_{Cu}'}}{\delta'} = \begin{cases} \frac{\sqrt{2} \cdot h}{\delta} = 2^{\frac{1}{2}} \cdot \phi \\ \frac{\sqrt{2} \cdot h}{2^{\frac{1}{2}} \cdot \delta} = \phi \end{cases} \quad (5.10)$$

5.1.3 Transformer

Similar considerations are done for scaling of a high frequency transformer. The allowed core and copper loss of the scaled transformer are assumed to be twice larger – $P_{Fe}'=2 \cdot P_{Fe}$ and $P_{Cu}'=2 \cdot P_{Cu}$. The area product formulation for a transformer is given by (5.11). Contrary to the dc inductor the transformer design is thermal limited most likely, thus reduction of the switching frequency enables increase of the flux density amplitude.

$$\begin{aligned}
 AP' &= \frac{P_t'}{k_{Cu} \cdot k_f \cdot \Delta B' \cdot J \cdot f_s'} = \\
 &= \begin{cases} \frac{2 \cdot P_t}{k_{Cu} \cdot k_f \cdot \Delta B \cdot J \cdot f_s} = 2 \cdot AP \\ \frac{2 \cdot P_t'}{k_{Cu} \cdot k_f \cdot \left(\frac{f_s}{f_s'}\right)^{\frac{\alpha}{\beta}} \cdot \Delta B \cdot J \cdot \frac{1}{2} \cdot f_s} = 4 \cdot \left(\frac{f_s}{f_s'}\right)^{-\frac{\alpha}{\beta}} \cdot AP = 2.83 \cdot AP \Big|_{\frac{\alpha}{\beta}=\frac{1}{2}} \end{cases} \quad (5.11)
 \end{aligned}$$

Of course there is a certain limit on the total core loss. If the switching frequency and the flux density are constant the core loss per volume unit remains the same and the required area product is twice larger (5.11). So, the core volume increases by factor of 1.68 according to (5.5) and the total core loss increases by the same factor. Growth of the area product in the second scenario depends on material properties. For $\alpha=1$ and $\beta=2$ the area product will increase by factor of 2.83 and the core volume will increase by factor of 2.18. In the second case reduction of the calculated flux density amplitude may be required in order to keep the total core loss on the allowed level. The flux density amplitude, the core volume and the total core loss are calculated iteratively.

However, the core loss isn't the only one loss mechanism in a transformer. Also copper losses, especially ac copper loss, is very important. Like it was previously with the transistor and the inductor scaling the resistance of the transformer winding has to decrease by half. Three variables decide about the dc resistance – the number of turns, the wire cross section area and MLT. MLT growth is given by (5.3) again. The number of turns (of the primary winding) is given by (5.12). In the first case only the core cross section area increases, while the allowed flux density and the applied volt-second remain constant. In the second case the applied volt-second value increases due to the switching frequency reduction. However, in the same time the allowed flux density amplitude increases (under assumption of constant specific core loss). Both variables have influence on the calculated number of primary winding turns and they counteract the applied volt-second increase. To keep the current density constant the wire cross section area increases twice. Resulting primary winding dc resistance is given by (5.13). In the first case the total copper area (the wire cross section area multiplied by the number of turns) increases with the same rate like the window area does, thus the copper fill factor in (5.11) doesn't change. In the first case the dc resistance decreases by more than half. In the second case the dc resistance change depends strongly on the required number of turns and thus it indirectly depends on the core

material properties. For assumed values of α and β the dc resistance increases faster than assumed thus a potential dc copper loss may become higher than expected.

$$n_1' = \frac{\lambda'}{A_c' \cdot 2 \cdot \Delta B'} = \begin{cases} \frac{\lambda}{2^{\frac{1}{2}} \cdot A_c \cdot 2 \cdot \Delta B} = 2^{-\frac{1}{2}} \cdot n_1 \\ \frac{2 \cdot \lambda}{2^{\frac{1}{2}} \cdot A_c' \cdot 2 \cdot \left(\frac{f_s}{f_s'}\right)^{\frac{\alpha}{\beta}} \cdot \Delta B'} = n_1 \end{cases} \quad (5.12)$$

$$R_{n1dc}' = \frac{n' \cdot \rho \cdot MLT'}{A_{Cu}'} = \begin{cases} \frac{2^{-\frac{1}{2}} \cdot n \cdot \rho \cdot 2^{\frac{1}{4}} \cdot MLT}{2 \cdot A_{Cu}} = \frac{R_{dc}}{2^{\frac{1}{4}}} \\ \frac{n \cdot \rho \cdot 2.83^{\frac{1}{4}} \cdot MLT}{2 \cdot A_{Cu}} = 0.65 \cdot R_{dc} \end{cases} \quad (5.13)$$

In a transformer however the ac resistance has a great importance. To keep the ac resistance low it's necessary to ensure a low dc resistance and a low ac to dc resistance factor F_R . For simplicity let's assume that a square wire is used and windings are interleaved, so only single layer solution is considered. Moreover, it's assumed that the original design had the relative penetration depth $\varphi=1$. Similarly to the inductor case discussed before, the relative penetration depth increases if the switching frequency remains constant. In such case the ac to dc resistance factor increases too. If the switching frequency decreases by half, the relative penetration depth remains constant, so the ac to dc resistance factor doesn't change.

$$\varphi' = \frac{h'}{\delta'} = \frac{\sqrt{A_{Cu}'}}{\delta'} = \begin{cases} \frac{\sqrt{2} \cdot h}{\delta} = 2^{\frac{1}{2}} \cdot \varphi \\ \frac{\sqrt{2} \cdot h}{2^{\frac{1}{2}} \cdot \delta} = \varphi \end{cases} \quad (5.14)$$

Using Dowell's method and curves presented on Figure 3.12 are used for estimation of the ac to dc resistance factor and the resulting ac resistance. So, in the first case the resulting ac resistance is 0.51 of the original one. In the second case the resulting ac resistance is 0.65 of the original one. However, if the number of layers in both designs increases to two the resulting ac resistance of the primary winding is 0.73 and 0.65 of the original ac resistance in the first and the second case respectively.

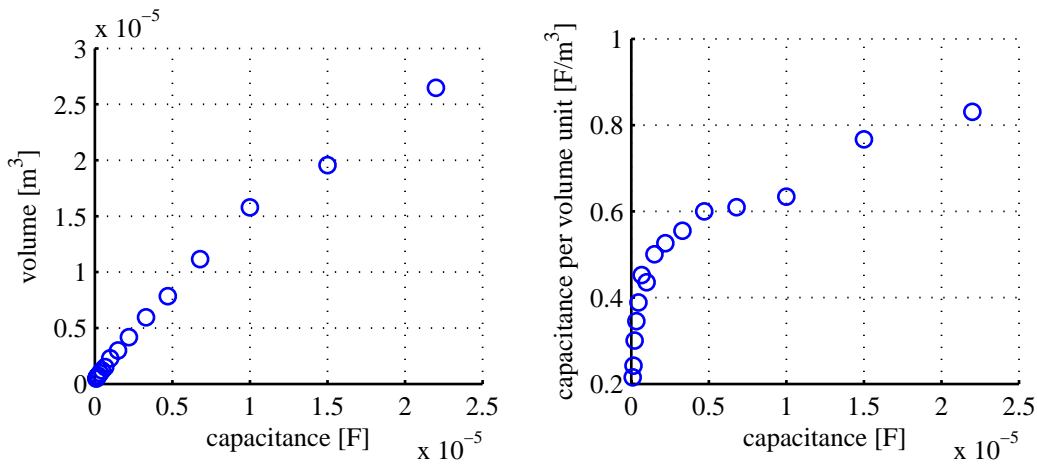


Figure 5.3 Volume and capacitance density vs. capacitance of 160 VDC film capacitors

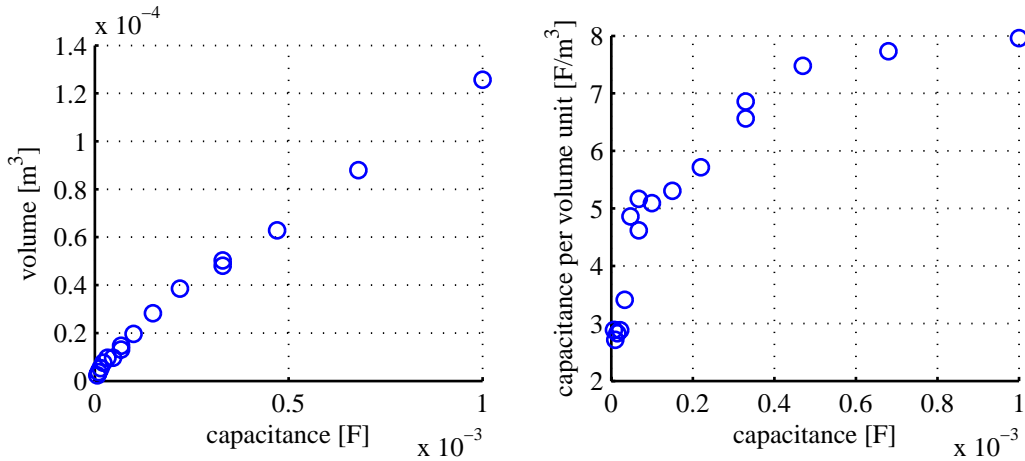


Figure 5.4 Volume and capacitance density vs. capacitance of 400 VDC aluminum electrolytic capacitors

5.1.4 Capacitor

Since the converter is scaled up in power only the voltage rating of used capacitors doesn't change. To keep the output voltage ripple on acceptable level the required capacitance is given by (5.15) in general case. In the first case, the required capacitance increases twice due to twice larger discharge current I_{out} . In the second case the required capacitance is four times larger than the original one due to a larger discharge current I_{out} and a longer discharge time (lower switching frequency f_s). Figure 5.3 presents relation between the volume (size) and the capacitance of several 160 VDC capacitors. Figure 5.4 presents the same relationship for 400 VDC capacitors.

$$C_1 = \frac{I_{out} \cdot D}{2 \cdot \Delta v_{out} \cdot f_s \cdot N} \quad (5.15)$$

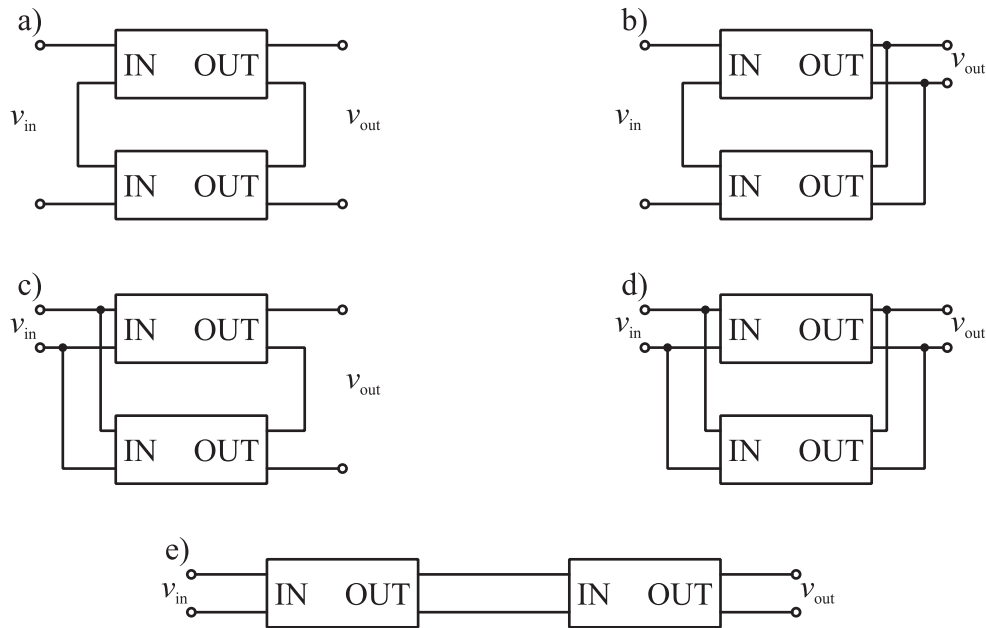


Figure 5.5 Possible modules interconnections: a) series-input series-output; b) series-input parallel-output; c) parallel-input series-output; d) parallel-input parallel-output; e) series connection of modules

5.2 Overview on modules interconnection

Figure 5.5 presents possible connections of isolated single-input single-output converter modules [97]. Series-input series-output connection isn't a very common one. This kind of connection can be useful in high voltage converters, where converter modules share input and output voltages. It allows use of simple switches, rather than complex ones made out of series connected devices. Series-input parallel-output connection is desired for a step-down application, where a conversion ratio is high, i.e. single stage power supply for a microprocessor. Modules input terminals are series connected and share the input voltage, so low voltage switches may be used. Output terminals are parallel connected increasing the output current handling capability. Moreover, the voltage conversion ratio of a single module is significantly lower than the conversion ratio of the whole converter, so the overall performance may increase. Parallel-input series-output connection is suited for a step-up applications. A high input current splits and it's shared among several modules, while the output voltage is built-up from output voltages of modules. Again, the voltage gain of a single module is lower than the gain of a whole converter and it may turn into a better performance. Series connection of input or output terminals requires a careful control of voltage sharing to avoid failure. Redundancy implementation is possible but it requires smart

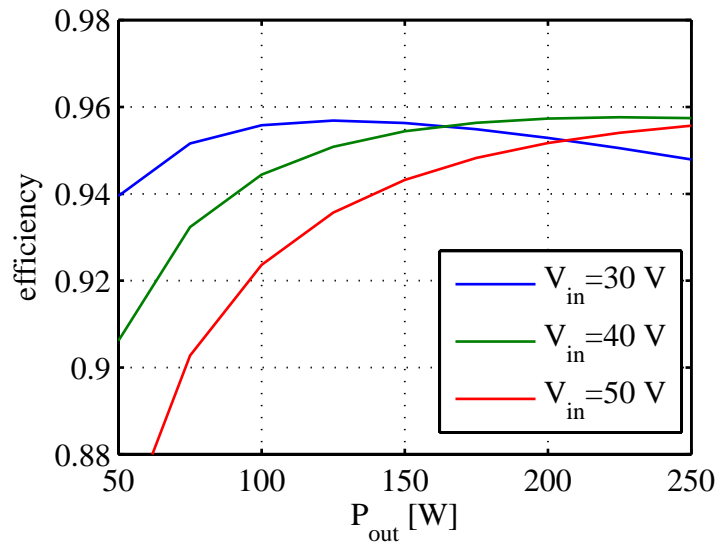


Figure 5.6 Estimated efficiency of a boost converter operating at different input voltages

protections and bypasses. However series connection of the input or the output requires a galvanic isolation, thus it's not feasible for a non-isolated converter.

Parallel-input parallel-output connection can be used for isolated and non-isolated converters. This kind of connection has no impact on voltage conversion ratio of a single module, but it enables easy extension of the power level. Moreover, using interleaving technique size of the input and the output filter may be reduced significantly, as described in paragraph 2.2.2.

Figure 5.5 e) presents series connected converters and it may be considered as a modular converter. This kind of converter is used in a multibus converter and in a converter with a very high conversion ratio. Use of this connection reduces voltage conversion ratio of each module and improves utilization of switches, as it was explained in paragraph 2.2.3. Also, presence of an intermediate bus improves power decoupling between the input and the output of the converter.

5.3 Fuel cell converter

Apart from loss mechanisms described in Chapter 3 and the converter design calculations presented in Chapter 4 total losses of a boost converter can be described by a function similar to the one given by (5.16). Exact values of particular coefficients depend on topology and components used. However, most likely the loss curve and the efficiency curve of a step-up converter will be similar to the one presented on Figure 5.6. Now, if the converter is optimized for the low input voltage, like it was presented in Chapter 4, the efficiency peaks at about half of the rated power. However, once the input voltage increases the efficiency peak moves toward higher power. Also, the peak efficiency will increase slightly in most cases. It's true for many isolated and non-isolated step-up converters and it has a great impact on the system performance.

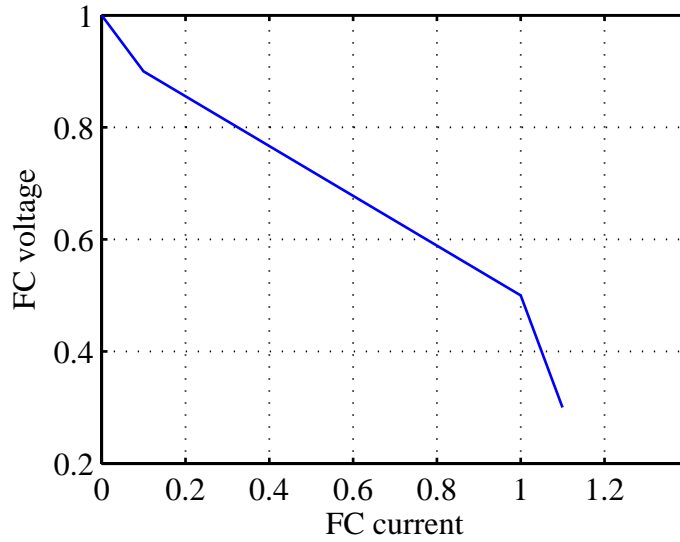


Figure 5.7 The fuel cell output voltage as a function of the fuel cell output current (example curve)

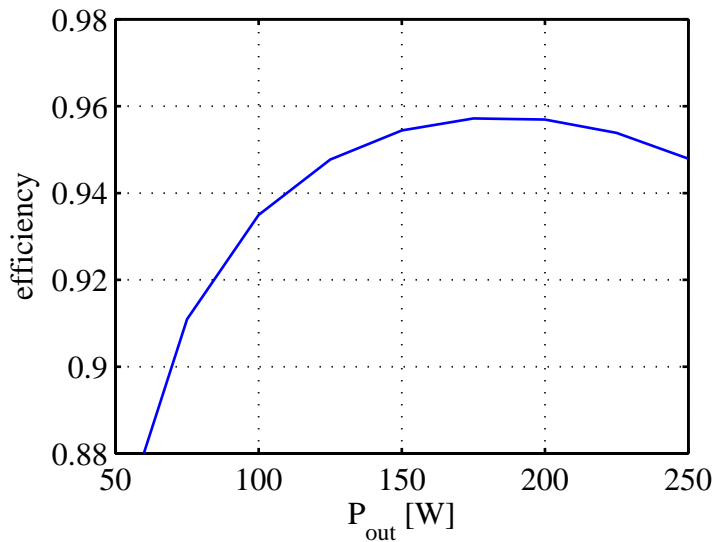


Figure 5.8 Estimated efficiency of a boost converter operating at variable input voltage (50 V at 50 W down to 30 V at 250 W)

$$\begin{aligned}
 P_{\text{loss}} &= f(V_{\text{in}}, I_{\text{in}}, V_{\text{out}}, I_{\text{out}}) = \\
 &= k_{V_{\text{in}}} \cdot V_{\text{in}}^{jV_{\text{in}}} + k_{I_{\text{in}}} \cdot I_{\text{in}}^{jI_{\text{in}}} + k_{V_{\text{out}}} \cdot V_{\text{out}}^{jV_{\text{out}}} + k_{I_{\text{out}}} \cdot I_{\text{out}}^{jI_{\text{out}}}
 \end{aligned} \tag{5.16}$$

Figure 5.7 presents the fuel cell voltage as a function of the fuel cell output current. It's just an example curve, but it indicates important feature of current fuel cells. At no load condition the fuel cell output voltage is the highest and it decreases while the fuel cell is being loaded. Now, the voltage / power profile is being combined with the step-up converter model and its efficiency curves from Figure 5.6. Efficiency of the converter is calculated for variable input voltage and the result is presented on Figure 5.8. At the rated output power and the minimum

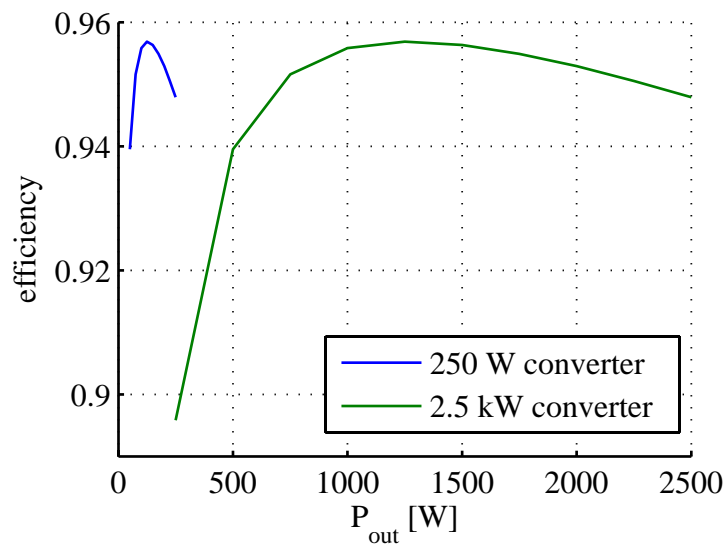


Figure 5.9 Estimated efficiency of the 250 W boost converter and the scaled 2.5 kW boost converter (ideal scaling) at 30 V input voltage

input voltage the power losses are dominated by conduction losses due to a high input current. At the other end, at light load the voltage dependant losses dominate, while the conduction losses are fairly low. An increased input voltage at light load leads to further rise of voltage dependant losses and efficiency degradation – compare curve on Figure 5.8 and curve related to 30 V input voltage on Figure 5.6.

5.4 Modular converter

As presented above a fuel cell output characteristic and a step-up converter characteristic doesn't match. It may result in worse poor utilization of converter performance in terms of the conversion efficiency, especially at light loads.

Use of a parallel-input parallel-output modular converter may help to overcome this drawback. Now, let's assume that the converter, which efficiency curves are presented on Figure 5.6 and Figure 5.8 is being scaled up in power – let's assume that the rated power of the new converter is 2.5 kW and the efficiency curve is "stretched" in power (ideal scaling), like presented on Figure 5.9. The peak efficiency in both cases is the same and it occurs at about half of the rated power (at the lowest input voltage). Also efficiency at rated power in both cases is the same.

Instead of scaling of the converter one may use ten smaller converters in parallel and achieve the same power level and the same efficiency profile like a single smaller converter has. Use of several paralleled converter modules requires careful current sharing – it includes both, control algorithm and current sensors in each module. On the other hand, using interleaving modulation scheme it's possible to reduce size of passive components, like the output capacitor or boost inductors. Moreover it's possible to improve converter efficiency for partial and light loads in compare with the scaled converter. Figure 5.10 presents estimated efficiency

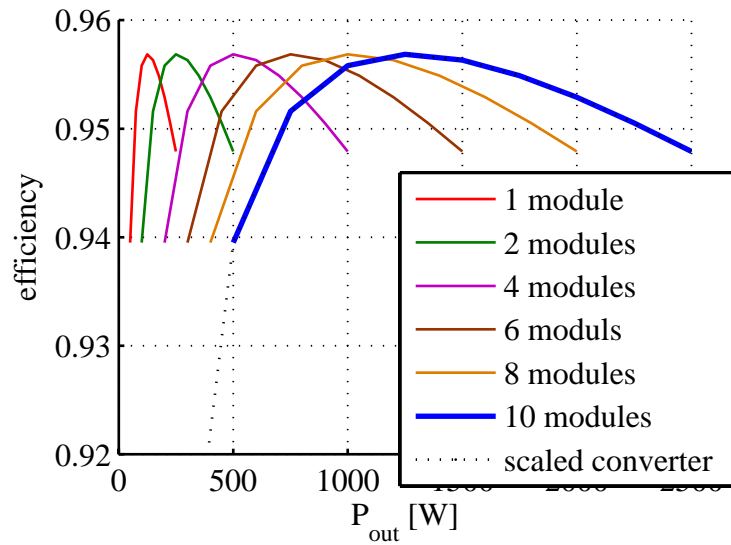


Figure 5.10 Estimated efficiency of the modular boost converter and the scaled converter operating with 30 V input voltage

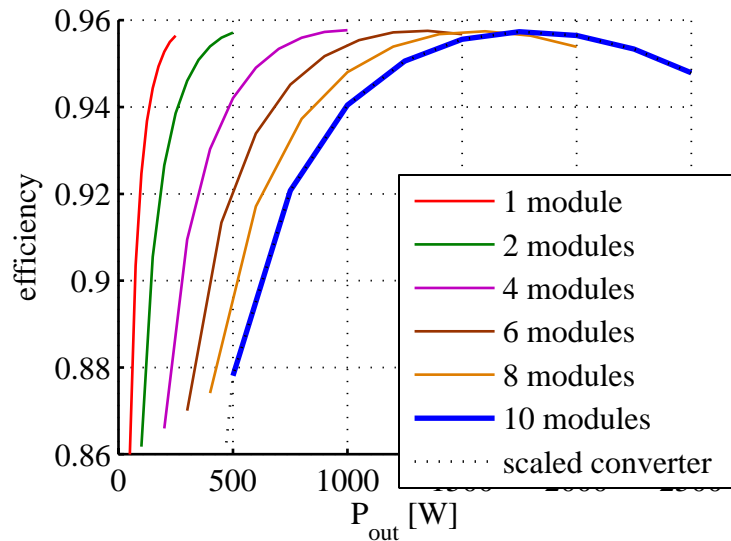


Figure 5.11 Estimated efficiency of the modular boost converter and the scaled converter operating with variable input voltage

curves for 2, 4, 6, 8, and 10 modules operating in parallel. In compare with the scaled converter (dashed curve on Figure 5.10) the modular converter performs better at partial and light loads. At the rated power efficiency of both converters is about the same.

If the input voltage is current dependent, like presented on Figure 5.7 use of the modular converter may provide even more benefits. Figure 5.11 presents estimated efficiency of the scaled converter and the modular converter operating at variable input voltage (different number of modules is turned-on).

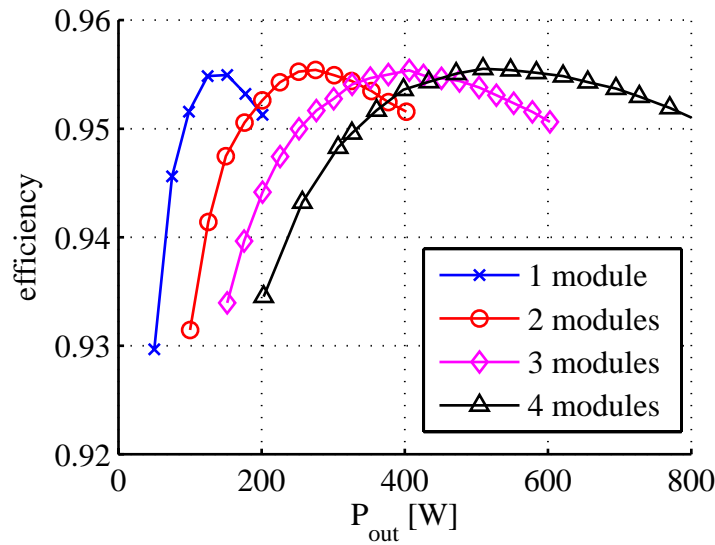


Figure 5.12 Measured efficiency of the modular boost converter operating at 30 V input voltage

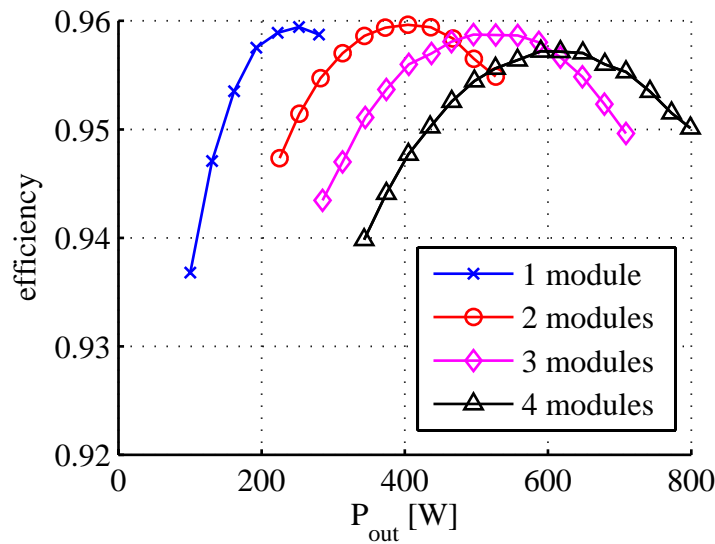


Figure 5.13 Measured efficiency of the modular boost converter operating at variable input voltage

To verify these considerations a 4-phase 800 W modular boost converter is built and tested. Figure 5.12 presents measured efficiency of the breadboard operating at 30 V input voltage and 400 V output voltage. It's demonstrated that the efficiency profile and the peak efficiency remain the same, regardless number of operating modules. Also, turning-off some of modules while the converter operates at light load actually improves efficiency, so it's possible to maintain a high efficiency over a wide load ranges.

Figure 5.13 presents measured efficiency of the breadboard operating at variable voltage – 50 V at 100 W output power drops down to 30 V at 800 W in linear manner. Now, efficiency of the modular converter actually increases when the

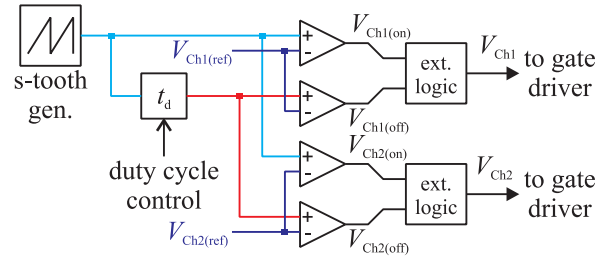


Figure 5.14 Block diagram of the proposed PWM generator

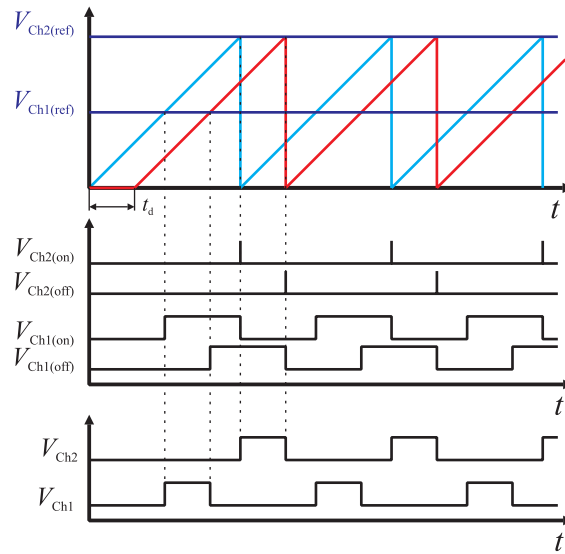


Figure 5.15 Key waveforms in the proposed PWM generator

output power decreases. It's opposite tendency in compare with a scaled boost converter.

5.4.1 Interleaved PWM generation

Described above method for efficiency improvement is valid aside from used modulation scheme – interleaved or synchronous. However, interleaving is preferred since it provide benefit of potentially smaller passive components. The challenge now is to get high quality multiphase gating signals which are interleaved equally, even if number of phases changes. So far no dedicated solution (like integrated circuit) was found on the market.

The solution proposed here bases on two sawtooth generators, the delay unit and set of comparators (two comparator per PWM channel), like presented on Figure 5.16. Figure 5.15 presents key waveforms. The delay unit delays the sawtooth signal by the programmable time t_d , which equals the transistor turn-on time. Each PWM channel has two comparators. One associated with original sawtooth signal and it's responsible for turn-on signal generation (rising edge of the comparator output). The other comparator is associated with the delayed sawtooth signal and it generates turn-off signal (rising edge of the comparator output). Basically both

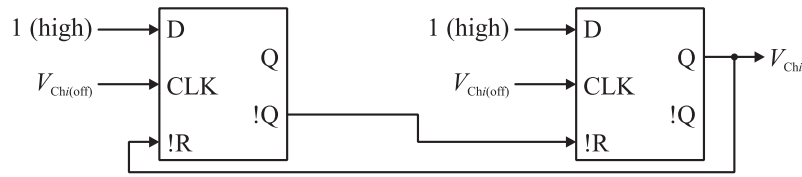


Figure 5.16 Diagram of external logic circuit

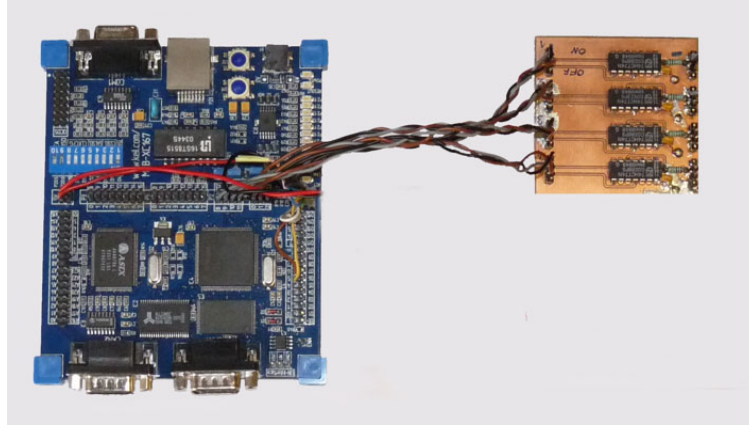


Figure 5.17 Picture of the XC167 board with external logic connected

comparators (in the same PWM channel) are connected to the same reference voltage $V_{Chi(ref)}$. Value of the reference voltage of the last PWM channel is just below the sawtooth peak voltage. Reference voltages of all remaining channels are proportionally lower, like presented on Figure 5.15. If number of active channels are about to change (increase or decrease) reference voltages are recalculated in the way that they are distributed uniformly from zero to the peak of the sawtooth signal. In this way all outputs are interleaved equally and have the same duty cycle, regardless the number of active channels. Additionally reference voltage of one comparator in a single channel may be changed and it results in duty cycle change in this channel. It can be used in an active current sharing scheme.

Since comparators provide only turn-on and turn-off signals it's necessary to process them further. Figure 5.16 presents a simple logic, based on two D-type flip-flops with asynchronous reset input, which detects rising edges of comparator outputs and process them into PWM waveforms.

The solution proposed here is implemented in microcontroller XC167CI-16F40F from Infineon [80]. This microcontroller provides 3+1 PWM channels, which unfortunately are desired to be part of 3-phase inverter (either grid connected or for electric drive). The microcontroller consists up to 32 capture-compare (CAPCOM) channels which are used for turn-on and turn-off signals generation as explained above. External D-type flip-flops (7474, dual in package) are used to get PWM waveforms. Figure 5.17 presents 4-phase implementation. C-code used in the microcontroller is available in Appendix B, paragraph B.12.

5.5 Summary

This chapter deals with scaling and paralleling of dc-dc step-up converters.

First scaling in power of the converter was discussed. It included considerations about use of higher power semiconductors and growth of passive components. Two cases were discussed in parallel – first, where the switching frequency didn't change after scaling of the converter, and the second, where use of a higher current rated transistors lead to the switching frequency reduction.

Next, impact of the variable input voltage on the converter efficiency was discussed based on the fuel cell converter example. It's found that at the light load (and high input voltage) the efficiency of the converter drops due to higher voltage dependent losses in the converter. On the other end, at the rated output power (and the lowest input voltage) conduction losses dominate in the converter. So, variable input voltage makes optimization of the converter more difficult.

Finally, the parallel modular converter concept was presented as an alternative for converter scaling. Intelligent use of the modular converter in fuel cell or similar applications may benefit in a better efficiency at medium and light loads in compare with the scaled converter.

Chapter 6

Experimental results

Some experimental results have been presented already. At the end of Chapter 3, in paragraph 3.8 the power loss model was verified using the boost converter breadboard (rated power 200 W, input voltage 20-30 V, output voltage 90 V). In paragraph 5.4 performance of a modular converter was demonstrated using 4-phase 800 W boost converter, which input voltage is 30-50 V and the output voltage is 400 V and it fits the specification from paragraph 1.4. Efficiency achieved by this converter was in the range of 95-96%.

To demonstrate performance of the push-pull-boost converter three breadboard based on this topology are built and tested. In this chapter experimental setup is presented first. It includes description of the equipment used, as well as presentation of three breadboards. Also electrical measurements of custom made magnetic components are presented. Then observed key waveforms and efficiency measurement results of all breadboards are presented and discussed briefly.

6.1 Experimental setup and breadboards

The diagram of the experimental setup used for efficiency measurement is presented on Figure 6.1 and the picture of the setup is presented on Figure 6.2. The converter under test (CUT) is supplied from the regulated dc power supply Toellner TOE-8872 (60 V, 65 A, 1500 W) [98]. The electronic load Zentro-Elektrik EL1000/800/20 (800 V, 20 A, 1000 W) [99] operating in current control mode is used. Auxiliary power supply GWINSTEK GPS-4303 (30 V, 3 A) [100] is used to power up gate drivers and microcontroller board (Infineon XC167 [80]), which is used as PWM gating signal generator. Use of the electronic load instead of variable resistors ensures more accurate control of the output power and improves system stability. Four precise 6 ½ digit multimeters Fluke 8845A [101] are used

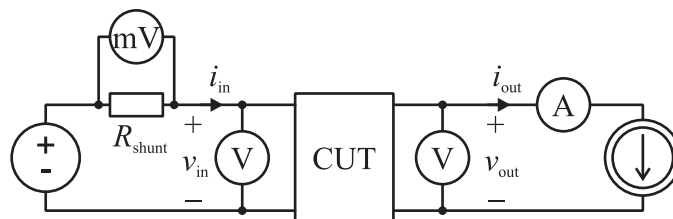


Figure 6.1 Diagram of the experimental setup

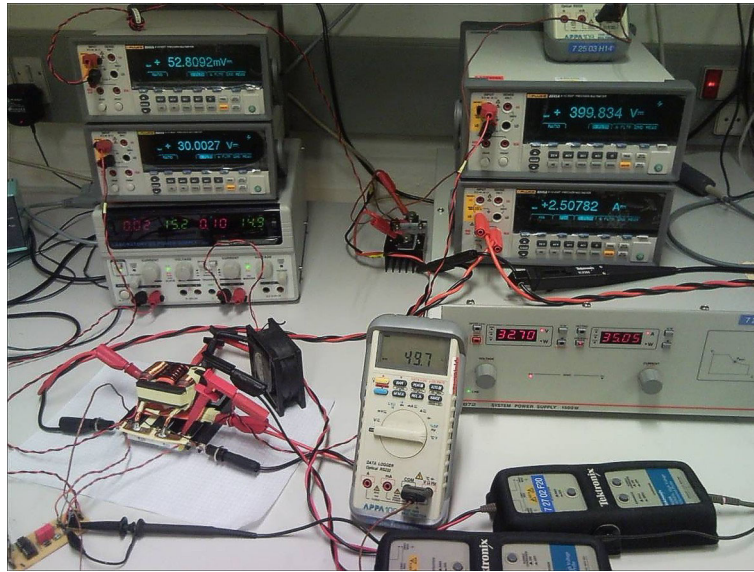


Figure 6.2 Picture of the experimental setup used

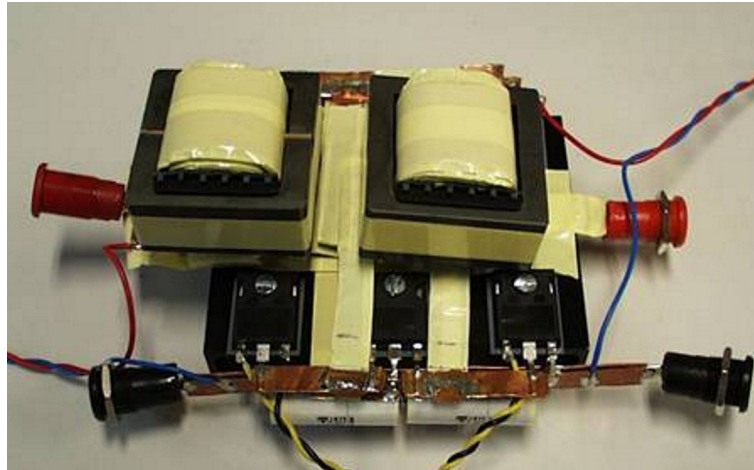


Figure 6.3 Picture of the 500 W push-pull-boost converter

for the input and output voltages and current measurements. All values, except the input current are measured directly. To measure the input current the precise 40 A / 60 mV shunt resistor is used. To improve thermal stability the shunt resistor is placed on the heatsink, so its temperature variations are greatly reduced. All measurements are done when the converter under test is warmed up. During measurement all multimeters are triggered synchronously, so influence of a low frequency changes is minimized.

Additionally, the digital scope Tektronix TDS-3014C [102] is used to observe and record waveforms. In connection with the digital scope high voltage differential probes Tektronix P5205 [102] and current probes Tektronix TCP-202 (15 A peak) [102] and LEM PR-50 (30 A peak) [103] are used.

Using this equipment three breadboards are tested. The first one is 500 W push-pull-boost converter made according to the design presented in Chapter 4. This converter has the dc inductor and the push-pull transformer arranged on two

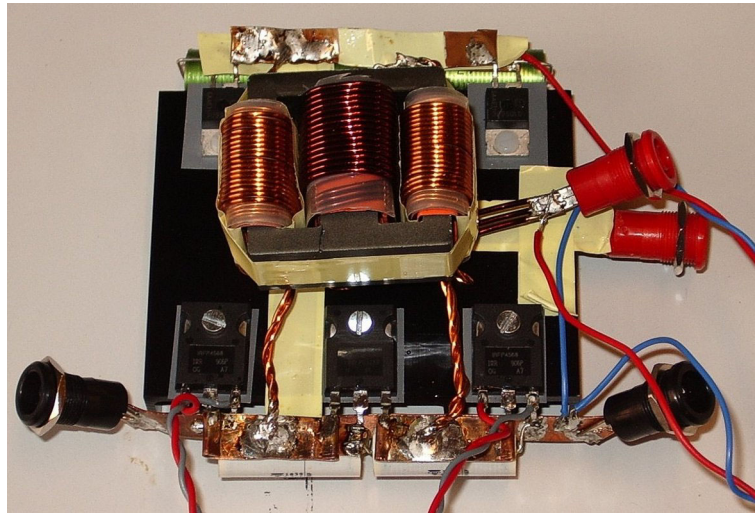


Figure 6.4 Picture of the 500 W push-pull-boost converter with integrated inductor-transformer

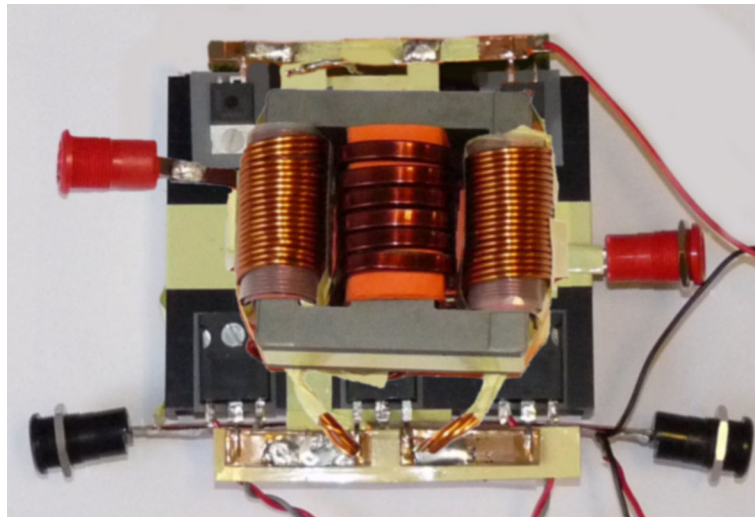


Figure 6.5 Picture of the 1 kW push-pull-boost converter with integrated inductor transformer

separate cores and the assembled converter is presented on Figure 6.3. More details about this breadboard is presented in Appendix A, paragraph A.4.

The second prototype is also 500 W push-pull-boost converter made according to the design calculations from Chapter 4. The difference is in magnetic components since this converter has integrated inductor-transformer. The assembled converter is presented on Figure 6.4. More details about this breadboard is presented in Appendix A, paragraph A.5.

The third breadboard is a scaled-up version of the second one. The scaling process is simplified and there are only two major changes in compare with the second breadboard – original transistors IRFP4321PbF [78] are replaced by newer ones IRFP4568PbF [78], which have lower on-state resistance, and integrated magnetic device is redesigned to handle higher power. Beside it, the switching

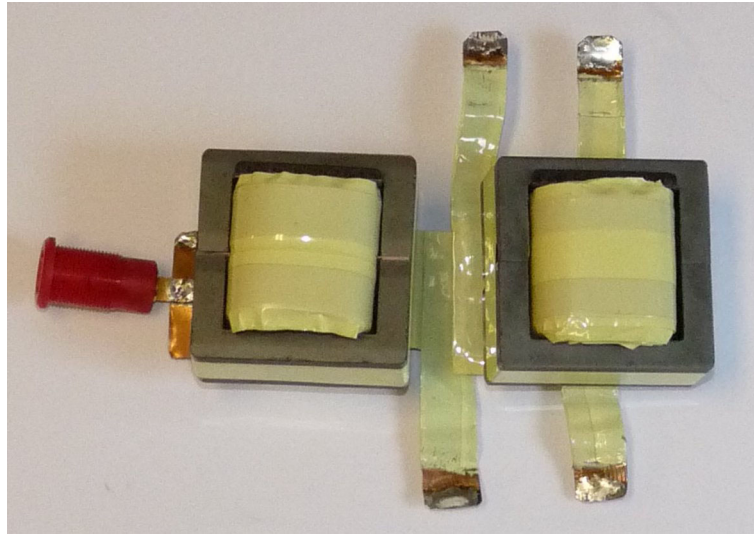


Figure 6.6 Picture of the assembled dc inductor and push-pull transformer for the 500 W push-pull-boost converter, cores size EE42/21/20

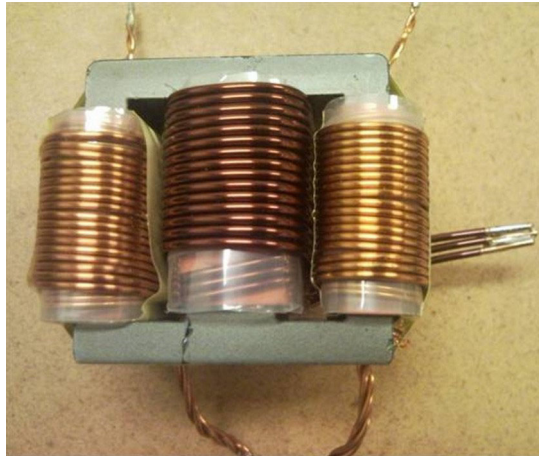


Figure 6.7 Picture of the assembled integrated inductor-transformer for the 500 W push-pull-boost converter, core size EE42/21/20

frequency remains the same, the diodes remain the same and the general converter layout remain the same too.

In addition to three breadboards presented above the 300 W push-pull-boost converter was made. This converter was the first breadboard with integrated inductor-transformer (EE42/21/20 core). More details about this breadboard is presented in Appendix A, paragraph A.3.

6.2 Magnetic components measurement

In Chapter 4 magnetic components for the push-pull-boost converter were designed. Their electrical parameters were found using FEMM simulation software. In this paragraph electrical parameters of these custom made magnetic components are measured using precise RLC-meter HP/Agilent 4284A. To make the comparison easier calculated and measured resistance values are presented as

Table 6.1 Calculated winding resistances of the dc inductor (core EE42/21/15) and the push-pull transformer

	Calculated	Measured
Resistance seen by the input dc current ($R_{L1}+R_{n1} R_{n11}$)	5.7 mΩ	-
Resistance seen by the input current ripple ($R_{L1}+R_{n1} R_{n11}$)	200 mΩ	-
Resistance seen by the secondary current ($R_{n2}+R_{n1}+R_{n11}$)	18.3 mΩ	-

Table 6.2 Calculated and measured winding resistances of the dc inductor (core EE42/21/20) and the push-pull transformer

	Calculated	Measured
Resistance seen by the input dc current ($R_{L1}+R_{n1} R_{n11}$)	3.8 mΩ	4.2 mΩ
Resistance seen by the input current ripple ($R_{L1}+R_{n1} R_{n11}$)	105 mΩ	120 mΩ
Resistance seen by the secondary current ($R_{n2}+R_{n1}+R_{n11}$)	18.3 mΩ	21 mΩ

Table 6.3 Calculated and measured winding resistances of the integrated inductor-transformer for the 500 W converter (EE42/21/20 core size)

	Calculated	Measured
Resistance seen by the input dc current ($R_{L1}+R_{n1} R_{n11}$)	6.3 mΩ	8 mΩ
Resistance seen by the input current ripple ($R_{L1}+R_{n1} R_{n11}$)	230 mΩ	290 mΩ
Resistance seen by the secondary current ($R_{n2}+R_{n1}+R_{n11}$)	71.9 mΩ	80 mΩ

Table 6.4 Calculated and measured winding resistances of the integrated inductor-transformer for the 1 kW converter (EE55/28/21 core size)

	Calculated	Measured
Resistance seen by the input dc current ($R_{L1}+R_{n1} R_{n11}$)	2.3 mΩ	2.8 mΩ
Resistance seen by the input current ripple ($R_{L1}+R_{n1} R_{n11}$)	180 mΩ	208 mΩ
Resistance seen by the secondary current ($R_{n2}+R_{n1}+R_{n11}$)	34.5 mΩ	40 mΩ

resistances seen by the particular current component, like explained in paragraph 4.1.3. The input current (dc and ac ripple) flows thru the inductor winding and thru primary windings which are effectively in parallel and the resistance seen by this current component is expressed as $R_{L1}+R_{n1}||R_{n11}$. The secondary winding current flows in the secondary winding, but it's also reflected to the primary windings, which are effectively series connected for this current component and the resistance seen by this current component is expressed as $R_{n2}+R_{n1}+R_{n11}$.

The dc inductor used in the first breadboard is different from the one designed in paragraph 4.2.5 since it bases on a larger core – EE42/21/20 instead of EE42/21/15. It results in lower number of turns and thus a lower winding dc resistance in compare with the design calculations in paragraph 4.2.5. The push-pull transformer made according to the design calculations from paragraph 4.2.4. Dc and ac resistances of both inductor designs are summarized in Table 6.1 and Table 6.2.

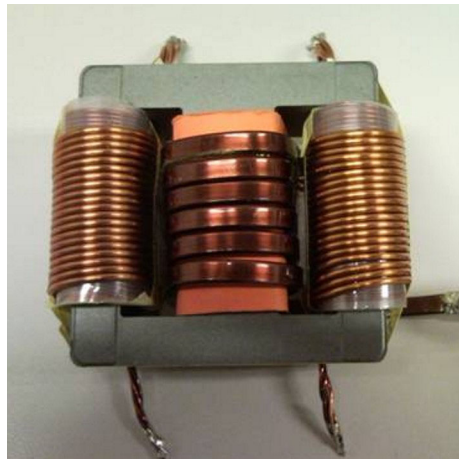


Figure 6.8 Picture of the assembled integrated inductor-transformer for the 1 kW push-pull-boost converter, core size EE55/28/21

Figure 6.7 presented assembled integrated inductor-transformer for the 500 W push-pull-boost converter made according to design calculations from paragraph 4.2.6. Table 6.3 summarizes calculated and measured winding resistances.

In addition, the integrated inductor-transformer has been scaled-up in the way that it's suitable for the 1 kW push-pull-boost converter. The assembled device is presented on Figure 6.8. It bases on EE55/28/21 core, ferrite material type P. Using the same guidelines like presented in paragraph 4.2.6 it's found that the inductor winding has 6 turns, the primary winding of the transformer has 8 turns and the secondary winding of the transformer has 18 turns. Calculated and measured winding resistances are summarized in Table 6.4.

6.3 Efficiency measurement and estimation

In this paragraph efficiency estimation and measurement results are presented. Figure 6.9 and Figure 6.10 present measured and estimated efficiency of the 500 W converter with separated inductor and transformer.

Figure 6.11 and Figure 6.12 shows measured and estimated efficiency of the 500 W converter with integrated inductor-transformer.

Figure 6.13 and Figure 6.14 shows measured and estimated efficiency of the 1 kW converter with integrated inductor-transformer.

All simulations were done under following conditions:

- temperature of all components was constant during all simulations
- the dc-bias and the temperature influence on the core loss was not included (certain coefficients in the model were set to zero)
- additional conduction losses caused by wiring and interconnections were not included
- calculated (not measured) values of winding resistances were used
- effect of the interwinding capacitance in case of the foil winding is not included

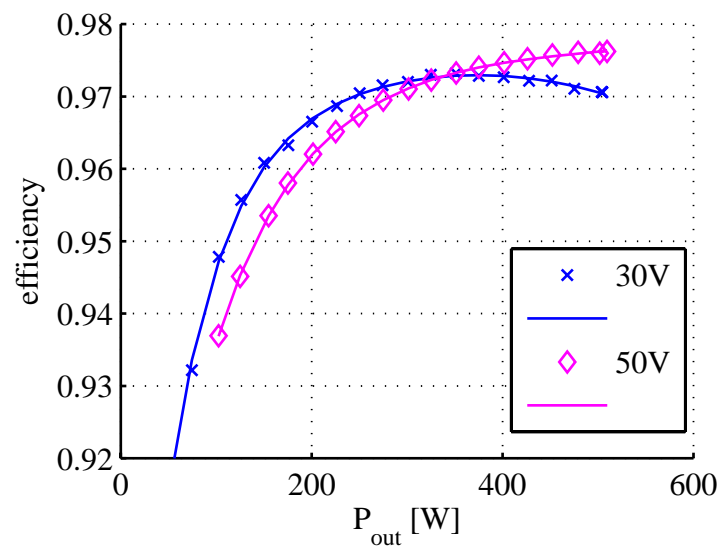


Figure 6.9 Measured efficiency of the 500 W push-pull-boost converter with separated inductor and transformer at 30 V and 50 V input voltage

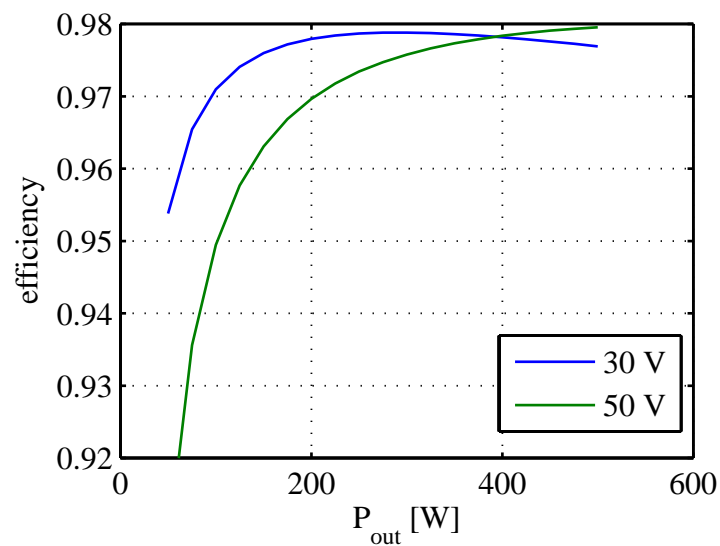


Figure 6.10 Estimated efficiency of the 500 W push-pull-boost converter with separated inductor and transformer at 30 V and 50 V input voltage

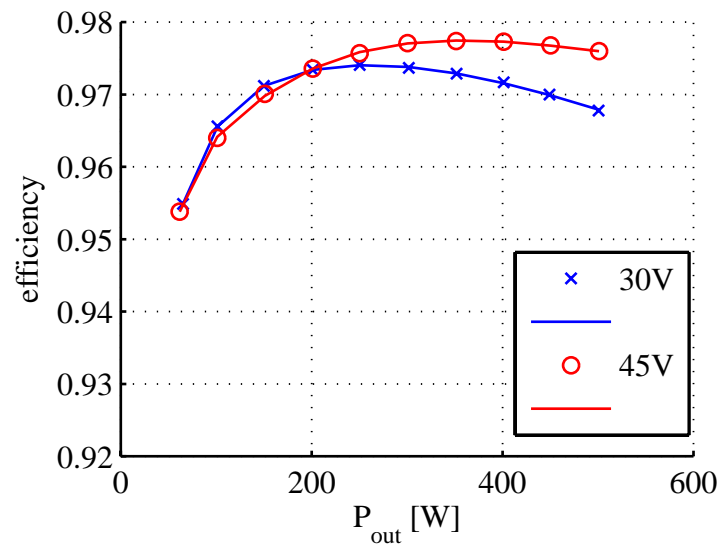


Figure 6.11 Measured efficiency of the 500 W push-pull-boost converter with integrated inductor-transformer at 30 V and 45 V input voltage

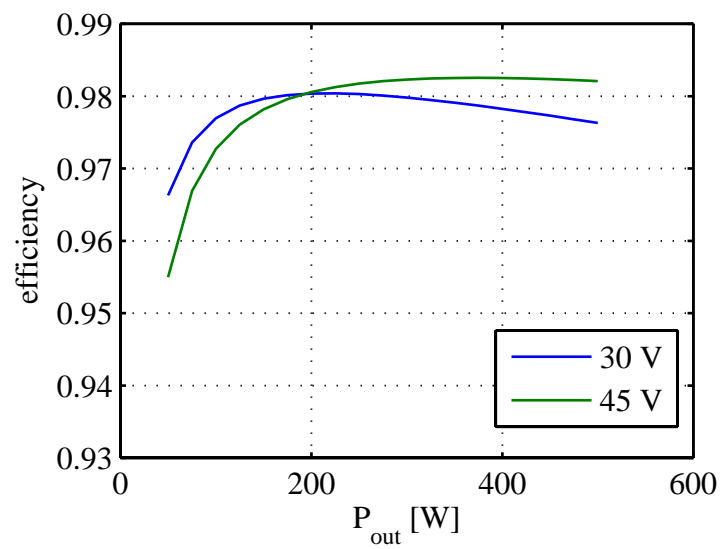


Figure 6.12 Estimated efficiency of the 500 W push-pull-boost converter with integrated inductor-transformer at 30 V and 45 V input voltage

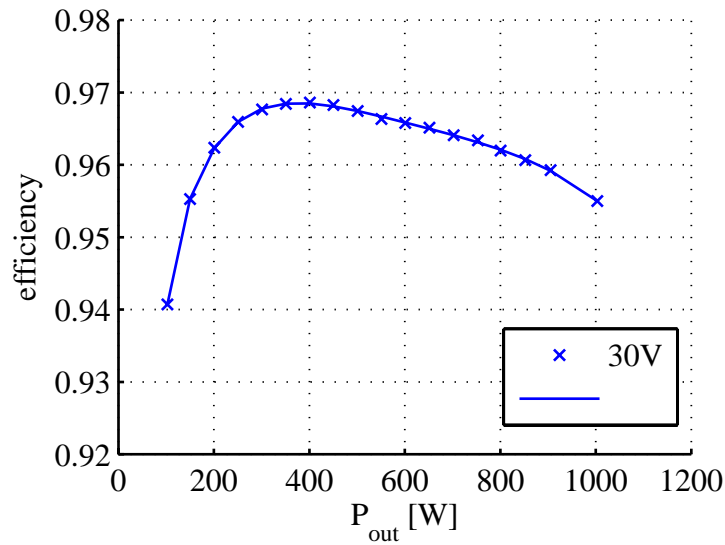


Figure 6.13 Measured efficiency of the 1 kW push-pull-boost converter with integrated inductor-transformer at 30 V input voltage

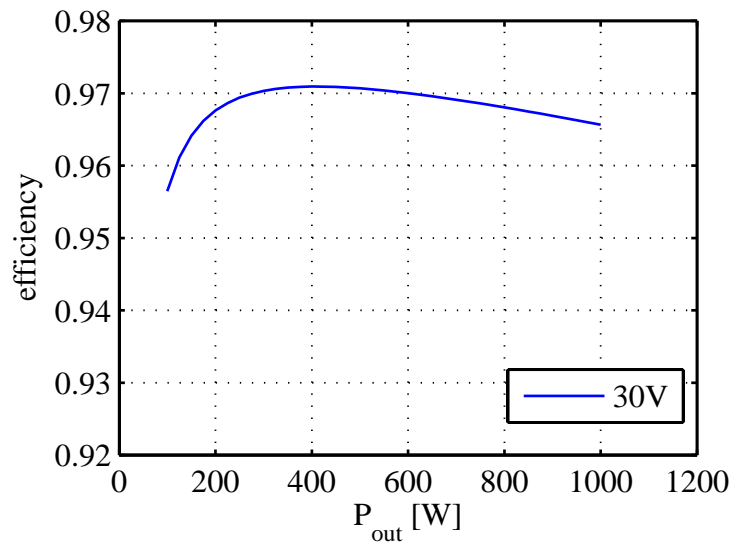


Figure 6.14 Estimated efficiency of the 1 kW push-pull-boost converter with integrated inductor-transformer at 30 V input voltage

6.4 Summary

In this chapter the experimental setup – equipments and breadboards – was presented and briefly described. Then estimated and measured values of winding resistance of magnetic components were provided. Finally, measured and estimated efficiency curves of three breadboards were presented.

Chapter 7

Conclusion

In this thesis non-isolated dc-dc step-up converters suitable for high voltage gain applications were investigated. At the beginning the literature study provided a good overview on different step-up topologies. It's found that converters based on an inductor and a coupled-inductor principle (a boost and a center tapped boost converters) as well as converters derived from isolated converters (a non-isolated flyback-boost, a non-isolated push-pull-boost and a non-isolated two-inductor-boost converters) are good candidates for future investigation. Description of selected topologies includes the circuit scheme, the diagram of key waveforms, the key equations as well as operation explanation and features of the converter. At the end of Chapter 2 all selected topologies are compared against each other in terms of required number of components and required ratings (current, voltage, etc.) of components. This quantitative comparison together with description indicated that the non-isolated push-pull-boost converter is the best candidate for the non-isolated fuel cell converter. Also the non-isolated two-inductor-boost converter is a very good candidate since it requires almost identical semiconductors and capacitors like the non-isolated push-pull-boost converter does. The main difference between these topologies is in magnetic components – the non-isolated push-pull-boost converter requires a smaller inductor, while the non-isolated two-inductor-boost converter requires a smaller and simpler transformer. Since a high efficiency is a main goal its important to predict losses in a converter in advance. So, modeling and calculation of losses is a very important part of the project. Used modeling approach and loss models are introduced and described in Chapter 3. Validation of these models is provided at the end of the Chapter based on the boost converter breadboard. In Chapter 4 the non-isolated push-pull-boost converter is being analyzed in details. Then the design example is provided to the reader. Also integration of the inductor and the push-pull transformer is presented in this Chapter. It's demonstrated that such integration of magnetic components on a single core may reduce size of the converter, while losses remain on the same level. In Chapter 5 converter scaling problem is presented. It includes discussion on growth of components and the impact on the converter operation and performance. Next modular converter approach is presented as an alternative for scaling. Based on simulations and measurements it's demonstrated that the efficiency of the modular converter remains high over wide range of loads. In case of the fuel cell application the efficiency of the modular converter increases while the output power decreases, which is exactly opposite in compare with a solid step-up converter. Finally, in Chapter 6 laboratory setup and equipment are described and experimental

results are presented. Three breadboards based on the non-isolated push-pull-boost converter topology are realized and tested demonstrating a very high efficiency, exceeding 97% in case of both 500 W breadboards.

7.1 Conclusions and new aspects

Below specific conclusions and novelties are summarized:

- It's found that a non-isolated push-pull-boost and a non-isolated two-inductor-boost topologies are the best candidates for a high voltage gain converters, including a fuel cell application. These topologies are more complex than a basic boost converter and they require more components, but they provide better utilization of switches and they require smaller passive components. Also these two topologies have a higher voltage gain, so they operate at a lower duty cycle than the basic boost converter does.
- It's demonstrated that a modular step-up converter may improve efficiency of the fuel cell converter. First, the converter design is not limited by the required output power, thus it's possible to utilize available components (especially MOSFETs) in optimum way ensuring low losses. Second, using a modular converter it's possible to improve efficiency at light and partial loads by turning-off one or more modules.
- It's demonstrated that a basic boost converter is able to achieve peak efficiency of 95.5%, which is well below level set by current state-of-the-art isolated converters (up to 98%) [104, 105]. However, using a proper non-isolated topology it's possible to achieve a similar performance in terms of the peak efficiency and the size of magnetic components. Integration of an inductor and a transformer on a single core enables further size reduction of magnetic components. It's believed that the limit of performance with available components was reached.
- Averaged steady-state models of converters together with component loss models is a useful tool in prediction of converter power losses. Component loss models base on parameters available in component datasheet in most cases, so parameters extraction is minimized or even avoided at all. With small changes in the main script file these models were used to estimate an optimum power level and an optimum switching frequency for a given MOSFETs. It's possible to develop similar averaged models for other topologies, including isolated dc-dc converter and inverters.
- It's believed that two dc-dc topologies developed during this project are novel. The first topology is so called a single switch dual output non-isolated boost converter and it was presented on 23rd Annual Applied Power Electronics Conference and Exposition APEC 2009, Austin, USA (see Appendix A.1). The second topology is a non-isolated two-inductor-boost converter (see paragraph 2.2.7) derived from an isolated two-inductor step-up topology.

Appendix A

Publications

A.1 A Single Switch Dual Output Non-Isolated Boost Converter (APEC 2008)

A Single Switch Dual Output Non-Isolated Boost Converter

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Abstract- There are many applications for high gain dc-dc converters. In several of these applications galvanic isolation is not required, but there are some safety issues regarding missing isolation and leakage current. Usage of a half-bridge inverter and a dual dc-link may solve this issues. In this paper very simple dual output non-isolated boost converter is presented. Single active switch is used to control both, positive and negative output voltages. The converter is desired to boost unregulated low input voltage 25-50 Vdc to regulated high voltage ± 400 Vdc in dual dc-link. In this paper proposed topology is analyzed and explained. Obtained experimental results prove good performance of the converter over wide range of input voltage and output power.

I. INTRODUCTION

Demand for high gain and high efficiency dc-dc converters is always present. Most recognized application for this kind of converters were UPS systems for network servers and telecom equipment. Nowadays new applications emerge: fuel cell (FC) and photovoltaic (PV) based distributed generators up to few kilowatts. Usually, in such cases, the low voltage from the dc source (25-50 Vdc) is converted to the higher dc-link voltage (350-400 Vdc) [1]. Nowadays many applications incorporates many smaller, paralleled and interleaved dc-dc converters instead of one large converter [2, 3]. The modular architecture provides better reliability, scalability, possibly higher efficiency and lower costs of production and maintenance. Also in some applications transformer-less converters are found as more efficient, smaller and cheaper solution. According to [4] usage of 3-level neutral-point-clamped (NPC) inverter is good choice in order to decrease leakage current to the ground and fluctuations of the PV panel in the non-isolated converter. In such solution one terminal of the source is connected to the grid neutral wire. On the other hand this solution requires positive and negative dc-link voltages. In [5, 6] there are presented non-isolated converters with dual (\pm) output.

In this paper a simple and efficient dual output non-isolated dc-dc boost converter is presented (Fig. 1). The proposed topology bases on the one presented in [7], but different connection of the secondary winding n_2 and voltage doubler (D_2, D_3, C_2, C_3) enables to generate positive and negative output voltage using only one active switch. This converter is a candidate for module in a parallel modular boost converter.

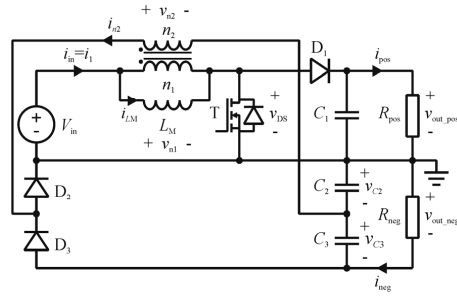


Fig. 1 - Proposed new single switch dual output boost converter

II. ANALYSIS OF THE PROPOSED CONVERTER

The proposed single switch dual output boost converter is presented on Fig. 1. In the simplest word, it is a basic boost converter [8] with very few additional components: a secondary winding n_2 (magnetically coupled with the primary winding n_1) and a voltage doubler (D_2, D_3, C_2, C_3). In a steady state voltage transfer functions of an ideal converter are given by (1). For $n_1=n_2$ and continuous conduction mode (CCM) the converter is able to generate symmetrical positive and negative voltages.

$$\begin{aligned} V_{out_pos} &= V_{in} \cdot \frac{1}{1-D} \\ V_{out_neg} &= V_{C2} + V_{C3} = \frac{n_2}{n_1} \cdot V_{in} + \frac{n_2}{n_1} \cdot \frac{D}{1-D} V_{in} \end{aligned} \quad (1)$$

For a little more detailed analysis it is assumed that both (positive and negative) loads are resistive and balanced. The coupled inductor is modeled as a two-windings ideal transformer with unity turns ratio ($n_1=n_2$) and a magnetizing inductor L_M in parallel to the primary winding. Leakage inductances L_{s1} and L_{s2} are very small and it's influence is negligible, however winding resistances R_{s1} and R_{s2} are taken into account. Diodes are modeled as an ideal diode in series with voltage source (forward voltage V_{Di} , $i=1, 2, 3$) and resistor (forward resistance R_{Di} , $i=1, 2, 3$). As long as SiC

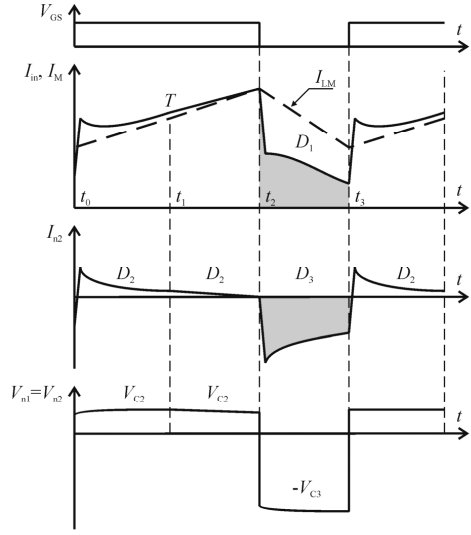


Fig. 2 - Operational waveforms

diodes are used no reverse recovery phenomena is considered. Moreover it is assumed that capacitors C_1 and C_3 have equal capacitances. Capacitor C_2 has a capacitance significantly larger than C_3 has. The converter operates in the continuous conduction mode (CCM). Under above assumptions there are four operational states. Basic waveforms are presented on Fig. 2.

State 1 (t_0-t_1): At the beginning of this state the transistor T is being turned-on. During this period the input voltage V_{in} is applied to the primary winding, the magnetizing current $i_{LM}(t)$ is rising linearly and the energy is stored in the magnetizing inductance L_M . A voltage slightly lower than the input voltage induces in the secondary winding n_2 and the current i_{n2} ramp-up to zero amps. Diode D_3 become reverse biased. If the voltage across capacitor C_2 is lower than the induced voltage $v_{n2}(t)$, then diode D_2 become forward biased and the capacitor C_2 being charged. The converter configuration is presented on Fig. 3a. If leakage inductances are very small and negligible, then i_{n2} current in time period t_0-t_1 is given by (2). In order to make the equation easier to read all resistances are grouped as a primary side resistance $R_{pri}=R_{s1}+R_{DSon}$; and a secondary side resistance $R_{sec}=R_{s2}+R_{D2}$. It is important to note that the magnetizing current $i_{LM}(t)$ is time dependent value and it has influence on charging the capacitor C_2 . Because $v_{C2}(t)$ voltage ripples are much smaller than the average output voltage V_{out_neg} it is assumed that output current I_{neg} is constant in time period t_0-t_1 .

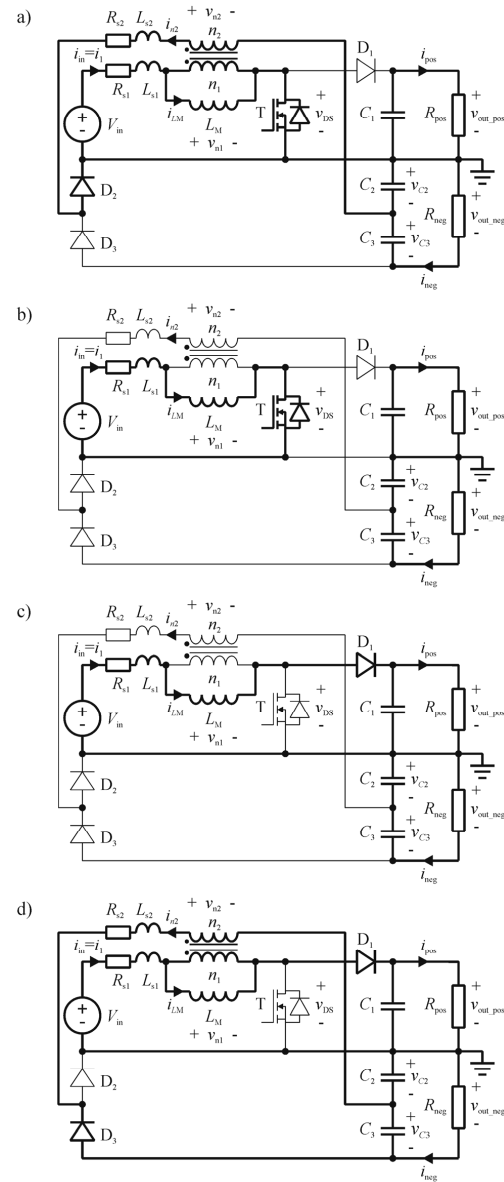


Fig. 3 - Basic operational states of the converter

$$i_{n2}(t) = \left(\frac{V_{in} - i_{LM}(t) \cdot R_{pri} - v_{C2}(t_0) - V_{D2}}{R_{pri} + R_{sec}} \right) \cdot \exp\left(\frac{-t}{(R_{pri} + R_{sec}) \cdot C_2}\right) + I_{neg} \quad (2)$$

State 2 (t_1 - t_2): In this state the transistor remains turned-on. Capacitor C_2 become fully charged and secondary winding current i_{n2} falls to a small value, about I_{neg} . In the same time the voltage drop on primary side resistances (R_{s1} , R_{DSon}) become larger due to the rising magnetizing current $i_{LM}(t)$ (3). It means that slightly lower voltage is applied to the ideal transformer's primary winding n_1 , lower voltage induces in the secondary winding n_2 and lower voltage is applied to the capacitor C_2 . If $i_{n2}(t)$ current become smaller than I_{neg} load current then the capacitor C_2 discharges through the load resistor R_{load_neg} and voltage $v_{C2}(t)$ falls too. Falling $v_{C2}(t)$ voltage drives current $i_{n2}(t)$ to rise. In many cases it may happen that voltage $v_{n1}(t)$ drops faster than voltage $v_{C2}(t)$ and current $i_{n2}(t)$ falls to zero. Both diodes D_2 and D_3 are reverse biased. The converter is in the state presented on Fig. 3b.

$$v_{n1}(t) \approx V_{in} - (R_{s1} + R_{DSon}) \cdot i_{LM}(t) \quad (3)$$

$$v_{C2}(t) \approx v_{C2}(t_1) - \frac{I_{neg} - i_{n2}(t)}{C_2} \cdot t \quad (4)$$

State 3 (t_2 - t_3): At the beginning of this state the transistor T is being turned-off. At the beginning the whole input current flows through D_1 diode to the capacitor C_1 . The voltage $v_{n1}(t)$ in t_2 moment is given by (5). Current flow in the converter is presented on Fig. 3c.

$$v_{n1}(t_2) = V_{out_pos} - V_{in} - i_{in}(t_2) \cdot (R_{s1} + R_{D1}) \quad (5)$$

If the voltage given by (5) is higher than C_3 capacitor voltage then the diode D_3 become forward biased and starts to conduct (Fig. 3d). The current in secondary winding is given by (6). Energy stored in the magnetizing inductor is transferred to output capacitors C_1 and C_3 . An amount of energy transferred to each capacitor depends on the load connected to each output and it's represented by a shaded areas on Fig. 2.

$$i_{n2}(t) = \frac{v_{n1}(t_2) - v_{C3}(t_2) - V_{D3}}{R_{s2} + R_{D3}} \cdot \exp\left(\frac{-t}{(R_{s2} + R_{D3}) \cdot C_3}\right) + I_{neg} \quad (6)$$

Now, let's assume that the converter operates with a very high duty cycle. It may happen that the transistor turn-off time become so short, capacitor C_3 cannot be fully recharged and its voltage $v_{C3}(t)$ at the beginning of the next switching period is lower. Consequently $v_{C3}(t)$ at the end of next period

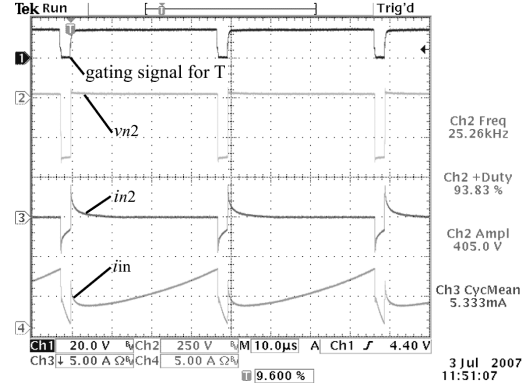


Fig. 4 - Observed waveforms

is lower than it was at the end of previous period. It means that difference between induced voltage $v_{n2}(t_2+T)$ and capacitor voltage $v_{C3}(t_2+T)$ become larger. The larger voltage difference will cause higher charging current. New equilibrium will be established, but by a cost of a lower average V_{C3} voltage.

III. EXPERIMENTAL SETUP AND RESULTS

In order to verify proposed idea the 200 W demonstrator converter has been built and tested. Desired input voltage range is 25-50 Vdc and it fits output voltage of the fuel cell stack up to few kW, single PV panel or many of lead acid batteries. The output voltage is ± 400 Vdc (dual dc-link) and it is suitable for half bridge 1-phase inverters and 3-phase 4-wires inverters. The converter was designed to operate at switching frequency $f_s=30$ kHz, but it was tested at switching frequencies from 25 kHz up to 35 kHz. A single 600 V MOSFET (Fairchild, FCH47N60) and two 600 V SiC diodes (Infineon, SDT05S60) are used (D_1 , D_3). Diode D_2 is silicon ultra fast diode 15ETL06 from International Rectifier. Due to the converter inherent properties this diode has no reverse recovery problem and it was chosen because of its low forward voltage drop. The coupled inductor bases on the toroid powder core (Magnetics, KoolMu 77930). It has 51 turns primary and 51 turns secondary winding.

Fig. 4 shows observed waveforms of the operating converter for minimum desired input voltage 25 Vdc (duty ratio equal to 93.8% at $f_s=25$ kHz) and 100 W output power. One may compare these waveforms with theoretical ones presented on Fig. 2. First of all it is important that i_{n2} (Ch3) current slopes are very steep during transistor transients. It means that leakage inductances are fairly small, like assumed before. Also a positive part of the observed current i_{n2} falls exponentially almost to zero value. Capacitor C_2 is fully charged. However negative part of the current i_{n2} does not fall to zero – as explained before the turn-off time is too short and capacitor C_3 cannot be fully recharged.

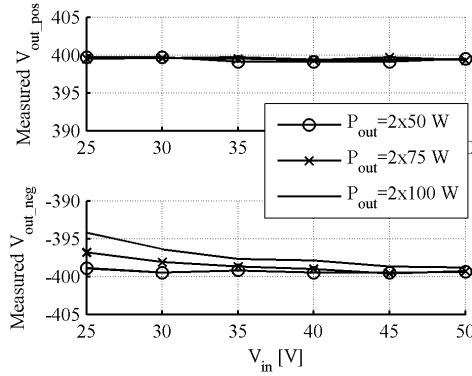


Fig. 5 - Measured output voltages (fs=25 kHz)

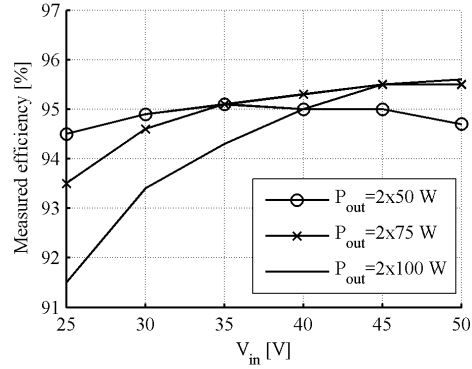


Fig. 7 - Measured efficiency of the converter (fs=25 kHz)

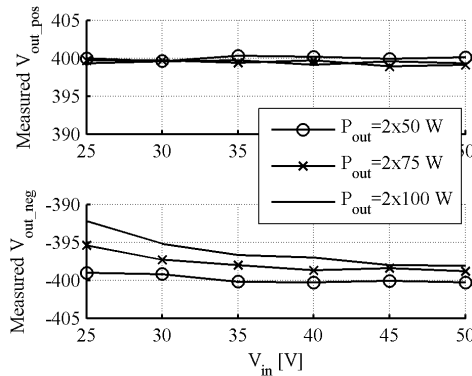


Fig. 6 - Measured output voltages (fs=30 kHz)

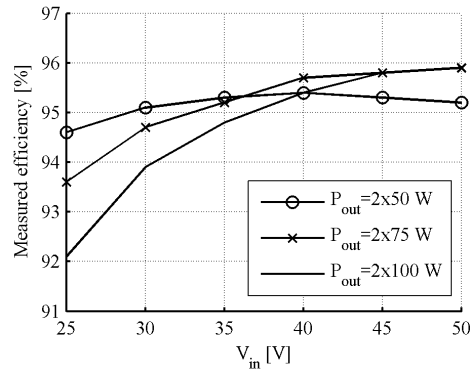


Fig. 8 - Measured efficiency of the converter (fs=30 kHz)

In fact, for lower input voltage V_{in} , negative output voltage V_{out_neg} 'drops' (Fig. 5). It is more visible at higher power and higher current. One explanation for this may be a greater influence of the parasitic components. Another one is a fact that a larger amount of energy has to be transferred to capacitor C_3 in each cycle. Comparing Fig. 5 and Fig. 6 one may notice that for higher switching frequency voltage asymmetry become larger, especially for lower input voltage and higher output power. On the other hand, by comparing Fig. 7 and Fig. 8 one may notice that for higher switching frequency an efficiency of the converter is higher. It's also important that for lower voltage (and higher input current) efficiency drops due to the conduction losses. For 100 W output power and high voltage efficiency drops a little also. It's mainly due to the core losses in the coupled inductor.

IV. CONCLUSION

In this paper new solution for a single-switch dual-output non-isolated boost converter is presented. This is a very

simple topology with low overall component count. The negative voltage is generated using the coupled inductor and the voltage doubler.

Analysis of the ideal converter was presented and principle of operation was explained. This analysis proved, that it is possible to create symmetrical output voltage over a wide range of the input voltage.

Finally experimental data were presented. Recorded waveforms confirmed principle of operation of the converter, but also indicated influence of parasitics. Measured output voltages pointed a potential limitation of the voltage gain.

ACKNOWLEDGMENT

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REFERENCES

- [1] Z. Qun, T. Fengfeng, and F. C. Lee, "A front-end DC/DC converter for network server applications," in *Power Electronics*

- Specialists Conference, 2001. PESC. 2001 IEEE 32nd Annual*, 2001, pp. 1535-1539 vol. 3.
- [2] V. Dang Bang, Y. Lembeye, J. P. Ferrieux, J. Barbaroux, and Y. Avenas, "New high power - high ratio non isolated DC-DC boost converter for Fuel cell applications," in *Power Electronics Specialists Conference, 2006. PESC '06. 37th IEEE*, 2006, pp. 1-7.
- [3] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," *Industry Applications, IEEE Transactions on*, vol. 41, pp. 1292-1306, 2005.
- [4] T. Kerekes, R. Teodorescu, and U. Borup, "Transformerless Photovoltaic Inverters Connected to the Grid," in *Applied Power Electronics Conference, APEC 2007 - Twenty Second Annual IEEE*, 2007, pp. 1733-1737.
- [5] Y. Kanthaphayao and C. Boonmee, "Dual-output DC-DC power supply without transformer," in *TENCON 2004. 2004 IEEE Region 10 Conference*, 2004, pp. 41-44 Vol. 4.
- [6] F. L. Luo, "Double-output Luo converters, an advanced voltage-lift technique," *Electric Power Applications, IEE Proceedings -*, vol. 147, pp. 469-485, 2000.
- [7] B. Ju-Won, R. Myung-Hyo, K. Tae-Jin, Y. Dong-Wook, and K. Jong-Soo, "High boost converter using voltage multiplier," in *Industrial Electronics Society, 2005. IECON 2005. 31st Annual Conference of IEEE*, 2005, p. 6 pp.
- [8] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power electronics : converters, applications, and design*, 3rd ed.: John Wiley & Sons, 2003.
- [9] J.-H. Kim and S.-K. Sul, "PWM Method of a Three-Level Neutral-Point-Clamped Converter under Neutral Point Imbalance Condition," in *Applied Power Electronics Conference, APEC 2007 - Twenty Second Annual IEEE*, 2007, pp. 1089-1094.
- [10] A. von Jouanne, D. Shaoan, and Z. Haoran, "A simple method for balancing the DC-link voltage of three-level inverters," in *Power Electronics Specialists Conference, 2001. PESC. 2001 IEEE 32nd Annual*, 2001, pp. 1341-1345 vol. 3.

A.2 Comparative Study on Paralleled vs. Scaled Dc-dc Converters in High Voltage Gain Applications (EPE-PEMC 2008)

Comparative Study on Paralleled vs. Scaled Dc-dc Converters in High Voltage Gain Applications

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Abstract—Today power converters are present in many commercial, medical and industrial applications. A lot of them are high power and high current applications. In order to increase power handling capability several transistors or diodes are paralleled often. However such paralleling may lead to converter's performance degradation or switches quick failure. A parallel modular converter built of many paralleled modules may be an interesting alternative, while a modular converter provides well known advantages like scalability, improved reliability and lower cost. This paper investigates possibility of improving an efficiency by intelligent usage of a modular boost converter in a high voltage gain application.

Keywords— DC power supply, Interleaved converters, Parallel operation, MOSFET

I. INTRODUCTION

If the power level is low it's possible to use only a single power semiconductor as a switch. For higher power levels a single transistor or a single diode may not be enough to handle high current and it is required to use bigger component or few ones in parallel. Usually it's easy to parallel two or three components, but for larger number of paralleled components interconnections become more complex. It's difficult to ensure equal stray inductances in each current path and some components may experience larger stress, especially during fast switching transients [1, 2]. In the same time due to on-state resistance mismatch and temperature rise current sharing problem between transistors may arise. Also there are some applications, e.g. UPS, solar inverters or drive inverters, in which basically the same converter topology is used for different power levels. Often in such case a basic converter is scaled up or down. This approach requires additional design work, more complex production, costly testing facilities and so on. One of disadvantages of a single converter is rather narrow range where high efficiency is achieved – a converter can be optimized for one operating point only. Optimization process is more complex if input voltage varies in a wide range, e.g. fuel cell applications.

A paralleling of whole dc-dc converters may be an alternative for paralleling or scaling of components inside a converter. This approach provides several, well known advantages. It includes expandability, higher reliability, easy maintenance and cheap production due to design standardization and mass production. Additionally, parallel modular converter provides more flexibility for a system designer and a customer. A system designer can

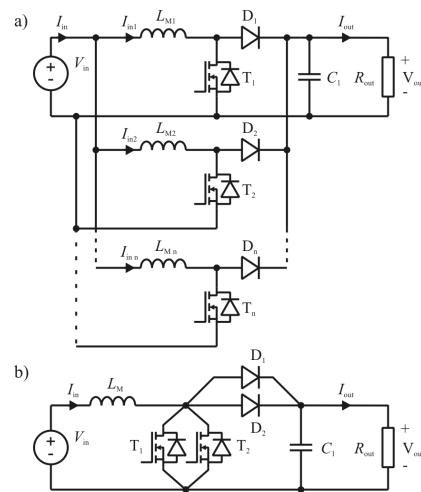


Fig. 1 - Parallel modular boost converter (a) and a boost converter with paralleled/scaled devices (b)

now design and optimize a converter for a power level which ensures the highest efficiency or the best components utilization. Further on, the system can be easily expanded by connecting more modules in parallel. It gives obvious benefits for a customer – instead of replacing whole system, it's necessary to add more modules. However paralleling of many modules creates new challenges. It may lead to unequal load sharing [3-7] or system instability [8-10].

This paper investigates possibility of improving the efficiency by intelligent usage of a modular boost converter in a high voltage gain application.

II. SCALING AND PARALLELING OF A BOOST CONVERTER

Fig. 1 presents a parallel modular converter (a) and a boost converter with paralleled semiconductors (b). Input and output voltages of both converters are the same and the difference is only in rated power of each one. The output power of a single module is limited by a current rating of used transistor – ideally a single module should consist only of one transistor and one diode – a device paralleling should be avoided. To increase power range several modules are paralleled and share the load.

Contrary to that approach Fig. 1 b presents a boost converter with paralleled and scaled devices. This converter consists of several paralleled transistors and diodes. Higher power level is achieved by redesigning the converter.

A. Power Semiconductors

In high power and high current applications the main switch is chosen to have sufficiently large current rating. However if such switch is not available or it's performance is not satisfactory then often practice is to parallel few transistors, split current between them and reduce total on-state losses. Paralleling of two or three transistors usually is relatively easy, but putting more devices in parallel may become a challenge – especially in medium/high frequency applications. One, but not the only one, difficulty is to ensure proper layout which provides equal current paths for all transistors – the same stray path length, the same stray inductance etc. During a transistor turn-on period energy is stored in the parasitic stray inductance (leads, connections etc.). When the transistor is being turn-off this energy is transferred between transistor's capacitance and the stray inductance causing oscillations. If there is an exact symmetry in the circuit each transistor absorbs the same amount of energy and experience the same oscillations. But in practice there are small differences e.g. due to component value tolerance or temperature difference. As it is stated in [2] such parameter differences may lead to unexpected oscillations in paralleled MOSFETs. In order to reduce oscillation different snubber circuits are used, but it increases component count and overall converter complexity. Handling of a high current by a switch composed of many devices can push the switching frequency down and result in more bulky passive components.

Also equal current sharing among several transistors is an important issue. As long as MOSFET transistors have a positive temperature coefficient they have an inherent self-balancing capability – up to some extend. Reference [1] analyzes these problems in details and introduces a dynamic current sharing from a gate side as a solution for a current sharing problem during on-state and switching periods. However this method bases on gate current control and may require additional components for a control circuit.

B. Growth of Passive Components

Not only transistor have to be rated for high current. Also all passive components have to be sufficiently large. In the literature one can find at least two approach for power inductor core size selection – one bases on core geometry factor K_g [11] and the other approach uses so called area product A_p [11, 12]. Area product for an inductor core is given by (1). Area product of a particular core can be found by multiplication core cross section area and window area (2).

$$A_p = \frac{L \cdot I_{dc} \cdot I_{max}}{B_{max} \cdot J \cdot K_u} [\text{cm}^4] \quad (1)$$

$$A_p = A_c \cdot W_a \quad (2)$$

References [11, 12] give a guidance about core scaling. Now, let's assume that the scaled boost converter has to process twice more power for the same input and output voltages and the same switching frequency. Thus the inductor dc current I_{dc} has to be twice larger. Assuming the same relative ripples $I_{pp\%}$ the peak current I_{max} will be twice larger too (3), but required inductance will be only half according to (4).

$$I_{max} = I_{dc} \cdot \left(1 + \frac{I_{pp\%}}{2}\right) \quad (3)$$

$$L = \frac{V_{in} \cdot D}{f_s \cdot I_{dc} \cdot I_{pp\%}} \quad (4)$$

By substituting new I_{dc} , I_{max} and L values to (1) one will find required area product A_p which is exactly twice larger than original one. Extending previous assumptions with constant peak induction B_{max} and constant current density J it's possible to find required number of turns and dc copper losses of the scaled inductor using (5) and (6) respectively. Mean length per turn growth rule is given by (7).

$$n = \frac{L \cdot I_{max}}{B_{max} \cdot A_c} \quad (5)$$

$$P_{dc} = I_{dc}^2 \cdot \frac{n \cdot MLT \cdot \rho}{A_{Cu}} \quad (6)$$

$$MLT = K_{MLT} \cdot A_p^{1/4} \quad (7)$$

It's found that a scaled inductor should have 0.707 number of turns of the original one and dc copper loss will increase by 68% only (under the assumption of optimum design and $P_{ic}=P_{cu}$ [11]). However under the same assumption of optimum design the current density has to decrease when the inductor is scaled up according to (9).

$$\text{surface} = K_s \cdot A_p^{1/2} \quad (8)$$

$$J = \frac{K_j}{A_p^{1/4}} \quad (9)$$

In the real world such ideal scaling is very rare, because of limited number of different core sizes. In many cases it results in a scaled component which is too bulky or not optimum.

Finally the output capacitor C_1 (Fig. 1) has to be sufficiently larger if the higher power has to be processed. Eq.(10) gives a required capacitance. It can be seen that for constant output voltage V_{out} , voltage peak-peak ripples $V_{pp\%}$, duty cycle D and switching frequency f_s the output filter capacitance C_1 is a directly proportional to the average output current I_{out} .

$$C_1 = \frac{I_{out} \cdot D}{V_{out} \cdot V_{pp\%} \cdot f_s} \quad (10)$$

Above assumptions will result in sufficiently larger output capacitor and greater capacitor rms current as well.

TABLE I – MODULE INPUT CURRENT DEVIATION UNDER NON-IDENTICAL MODULES OPERATION

	2 modules	4 modules	8 modules
R_s -20%	+4.7%	+7.1%	+8.4%
L_M -20%	0.0%	0.0%	0.0%
R_{DS} -20%	+5.2%	+7.9%	+9.3%
V_f -20%	+1.5%	+2.2%	+2.6%
R_f -20%	+0.8%	+1.1%	+1.3%
Worst case	+13.0%	+20.4%	+24.4%
Duty +0.1%	+32.1%	+40.4%	+53.5%

TABLE II – TRANSISTOR RMS CURRENT DEVIATION UNDER NON-IDENTICAL MODULES OPERATION

	2 modules	4 modules	8 modules
R_s -20%	+4.4%	+6.7%	+7.9%
L_M -20%	+1.7%	+1.7%	+1.7%
R_{DS} -20%	+4.8%	+7.4%	+8.8%
V_f -20%	+1.4%	+2.1%	+2.4%
R_f -20%	+0.7%	+1.1%	+1.2%
Worst case	+12.2%	+19.2%	+23.0%
Duty +0.1%	+30.4%	+44.0%	+50.9%

III. MODULAR POWER CONVERTER APPROACH

Paralleling of dc-dc converters is a well know technique for extending an output power and may be an interesting alternative for a large or scaled up converters with multiple paralleled transistors. This section gives an overview on few common issues and challenges related to paralleling of dc-dc converters.

A. Current Sharing

The most recognized is current sharing problem. If the single dc-dc module has relatively low power it is possible to relay on a simple droop method. Also most of paralleled converters has an inherent self-balancing functionality – up to some extent. If one of modules conducts higher current it heats up, so it's resistances increase and unbalance current is limited in this way. But if safety limits are lower or a single module has higher power then active current sharing method is required. Different paralleling and current sharing methods are presented in [3]. This paper describes several passive and active methods, including Master-Slave and Average Current Programming Methods. More details about active current sharing methods one may find in [4-7].

B. Instability of Paralleled Dc-Dc Converters

Another problem caused by paralleled dc-dc converters is potential system instability. The one reason for this is that dynamic of the parallel system is different that dynamic characteristic of a single converter. It means that a controller tuned for a single module may not work properly with paralleled converters leading to undesired system oscillations. The other reason for instability is presence of multiple current control loops which are introduced by some of current control sharing methods. This problem is widely discussed in [8-10].

IV. SIMULATION OF NON-IDENTICAL MODULES PARALLEL OPERATION

Due to potential current unbalance problem several simulations of non-identical modules are done using Matlab®/PLECS® software. Model parameters and

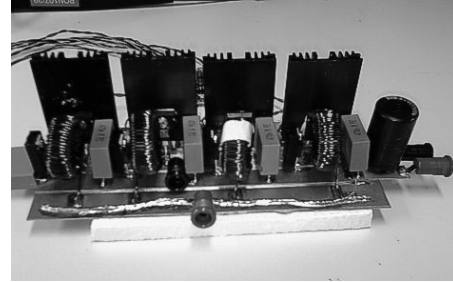


Fig. 2 - 4-phase modular boost converter

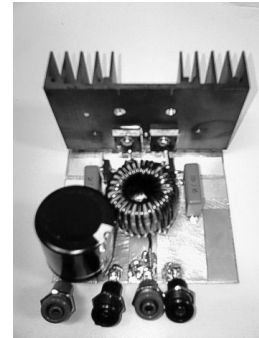


Fig. 3 - Scaled boost converter

components values are selected to fit a breadboard specification described in Section V.

First, simulation of 2, 4 and 8 paralleled identical modules (Fig. 1 a) operating in open loop configuration were performed. Results confirm stable operation and equal current sharing among all modules.

Second step is to simulate behavior of non-identical modules. It's done by changing component values in one of modules. Only one parameter at the time was changed in order to find out which parameter deviation introduces the largest current unbalance. Following parameters (component values) were decreased by 20%: inductor winding resistance R_s , inductance L_M , transistor on-state resistance R_{DS} , diode forward voltage V_f and diode forward resistance R_f .

Next, based on previous observations the 'worst case' scenario was simulated – all components values are increased or decreased by 20% to create the largest unbalance.

Finally, duty cycle value was increased by +0.1% in one of modules to create unbalanced conditions.

Simulation results are summarized in Table I and Table II, where module input current deviation and transistor rms current deviation are presented. It has been found that the inductor series resistance and transistor on-state resistance have big influence on current unbalance. Both resistances are located on low voltage and high current side of the converter. Also, the same disturbance results in larger unbalance when more modules are paralleled. However, the modular converter like this seems to be very

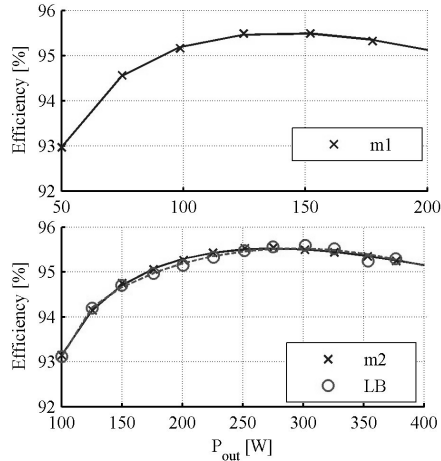


Fig. 4 - Efficiency of a single boost module (m1), two modules in parallel (m2) and the scaled converter (LB) at 30 V input voltage

sensitive to duty cycle unbalance – even a very small deviation in duty cycle may result in huge current unbalance. So, the special attention should be given to PWM gating signals and gate drivers' design.

V. EXPERIMENTAL SETUP

Two demonstrator converters are build and tested in order to compare their performance and efficiency.

A. Description of the Modular Converter

The first one is a modular boost converter built-up from four paralleled boost converter modules (Fig. 1 a, Fig. 2). Desired input voltage range is 30-50 Vdc and output voltage is regulated at 350 Vdc. A single 600 V MOSFET (Fairchild, FCH47N60) and a single 600 V SiC diode (Infineon, SDT05S60) are used. The storage inductor bases on a toroid powder core (Magnetics, High Flux 58071) and it has 68 turns winding. Maximum output power of a single module is 200 W and in fact it's limited

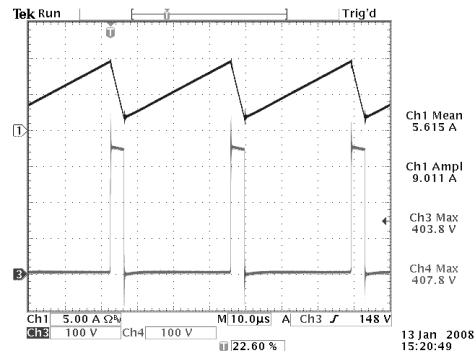


Fig. 5 - Input current (Ch1) and transistor drain-source voltage (Ch3, Ch4)

by MOSFET's conduction loss at the lowest input voltage. To achieve higher power level more identical modules are connected in parallel to the first one. Each transistor has its own gate driver and it's controlled by an individual signal. A single Infineon XC167 microcontroller is used for PWM generation. All PWM signals have the same duty cycle and they are equally interleaved – phase shift between PWM signals depends on number of operating modules and it's adjusted continuously.

B. Description of the Scaled Converter

The second converter is scaled up to 400 W version of a single 200 W boost module (Fig. 1 b, Fig. 3). It is designed to process twice larger power like the single module and achieve the same efficiency. This converter consist two paralleled MOSFETs and two SiC diodes – the same type like in the modular converter described above. Each transistor has its own gate driver, but PWM signal is common for both transistors. Both MOSFETs operate synchronously, so effective on-state resistance R_{DSon} is half of a single MOSFET resistance. Also it enables to process twice larger current. Due to higher current the inductor has to be redesign and scaled up – substituting new current and inductance values to (1) it's found that new core should provide twice larger area product value. There are at least three ways to achieve higher power handling capability of the inductor: 1) put two smaller inductors in parallel; 2) redesign an inductor using two stacked smaller cores; 3) redesign an inductor using one larger core. This converter has the storage inductor built on two stacked toroid cores (Magnetics, High Flux 58071). Based on area product approach it's found that such stacked cores have twice larger power handling capability (the same window area W_w , twice larger core cross section area A_c) and it fit's to requirements. Number of turns is decreased by half (34 turns) and, due to doubled core cross section area A_c , inductance of the inductor is decreased by half too. Specific core losses given by Steinmetz equation shall remain on the same level, but total core loss will be twice larger due to larger core volume. The winding wire size is selected in respect to required winding dc resistance, which should be half of dc resistance of the inductor in modular converter. For twice larger current it gives twice larger copper loss.

Using this design approach, the converter is expected to

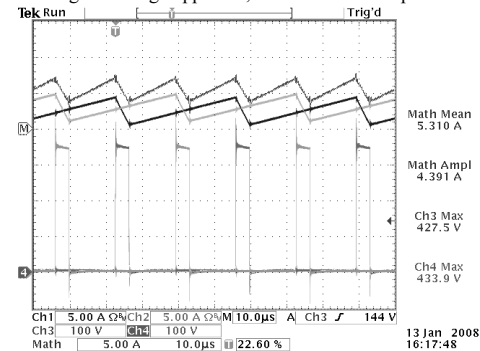


Fig. 6 - Module input currents (Ch1 and Ch2), converter input current (Math) and transistor drain-source voltages (Ch3 and Ch4)

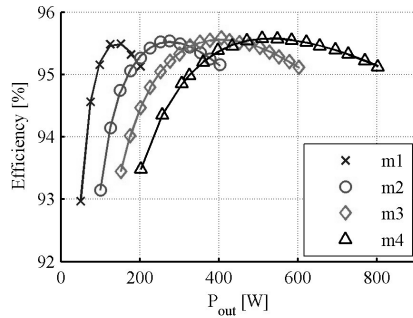


Fig. 7 - Efficiency of a modular converter at 30 V input voltage

have twice larger maximum power and similar efficiency to the single converter module described previously.

VI. EXPERIMENTAL RESULTS

At the beginning three converter configurations were compared in terms of achieved efficiency. At an input voltage of 30 V the single module (curve m1) efficiency was measured in the power range from 50 to 200 W. Next efficiency of a scaled 400 W boost converter (curve LB) was measured and compared with two paralleled modules (curve m2) under the same conditions (input voltage 30 V, output power 100-400 W). Results are presented on Fig. 4. One may observe that efficiency curves m1, m2 and LB are very similar – it means that the scaling process is done correctly. Also, it confirms that paralleling of two switches shall not affect the efficiency significantly.

Fig. 5 and Fig. 6 present input currents and transistor voltages of a scaled 400 W converter and two interleaved modules respectively. One may find that input current ripples are significantly lower for interleaved modular system. Moreover, output voltage ripples have a twice larger frequency, and it results in smaller output capacitor. Also it's should be emphasized that the parallel converter operates in open loop configuration and current sharing is very good in spite of absence of current controller.

Next the input voltage is set to 30 V and efficiency was measured for different number of modules (up to four modules in parallel) for different power levels. Results are presented on Fig. 7. By adjusting number of operating modules it's possible to keep high efficiency over a wide range of output power. By adding more modules it's easy to extend power level of the system.

Finally, measurements under variable input voltage were done. Variable input voltage simulates behavior of a PEM fuel cell – output voltage of the stack is highest at no-load condition and decreases while output power increases. In the lab setup input voltage was set to 50 V for 100 W and decreased linearly to 30 V at 800 W output power. Under such conditions the efficiency was measured for different number of modules. Results are presented on Fig. 8 together with input voltage value. One may observe that efficiency of four modules in parallel (curve m4) drops quickly while output power decreases, e.g. down to 94% at 340 W. In this case it's beneficial to turn-off one or two modules and increase

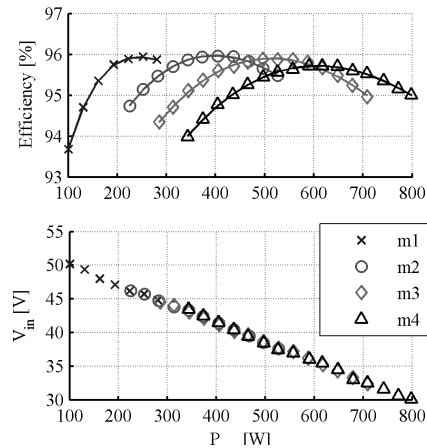


Fig. 8 - Efficiency of a modular converter at variable input voltage

efficiency of the whole system. One may observe that efficiency of such modular system increases while output power decreases – this behavior is opposite to most of traditional converters, where efficiency drops at low load.

VII. CONCLUSION

This paper gives an overview on scaling and paralleling of boost converters. Two demonstrator converters are built, tested and results are presented. Based on these results it's stated that modular converter gives more flexibility and provides additional degree of freedom for a system designer. Adjusting number of operating modules leads to optimum utilization of the converter. In case of a fuel cell application, with variable input voltage, the parallel converter provides high efficiency over a wide range of output power levels.

ACKNOWLEDGMENT

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REFERENCES

- [1] W. Hongfang and F. Wang, "Power MOSFETs Paralleling Operation for High Power High Density Converters," in *Industry Applications Conference, 2006. 41st IAS Annual Meeting. Conference Record of the 2006 IEEE*, 2006, pp. 2284-2289.
- [2] J. G. Kassakian and D. Lau, "An analysis and experimental verification of parasitic oscillations in paralleled power MOSFET's," *Electron Devices, IEEE Transactions on*, vol. 31, pp. 959-963, 1984.
- [3] L. Shiguo, Y. Zhihong, L. Ray-Lee, and F. C. Lee, "A classification and evaluation of paralleling methods for power supply modules," in *Power Electronics Specialists Conference, 1999. PESC 99. 30th Annual IEEE*, 1999, pp. 901-908 vol.2.
- [4] T. Kohama, T. Ninomiya, M. Shoyama, and F. Ihara, "Dynamic analysis of parallel-module converter system with current balance

- controllers," in *Telecommunications Energy Conference, 1994. INTELEC '94., 16th International*, 1994, pp. 190-195.
- [5] D. J. Perreault, R. L. Selders, and J. G. Kassakian, "Frequency-based current-sharing techniques for paralleled power converters," in *Power Electronics Specialists Conference, 1996. PESC '96 Record., 27th Annual IEEE*, 1996, pp. 1073-1079 vol.2.
- [6] N. Hur and N. Kwanghee, "A robust load-sharing control scheme for parallel-connected multisystems," *Industrial Electronics, IEEE Transactions on*, vol. 47, pp. 871-879, 2000.
- [7] D. J. Perreault, K. Sato, R. L. Selders, Jr., and J. G. Kassakian, "Switching-ripple-based current sharing for paralleled power converters," *Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on [see also Circuits and Systems I: Regular Papers, IEEE Transactions on]*, vol. 46, pp. 1264-1274, 1999.
- [8] H. H. C. Iu and V. Pjevalica, "Experimental study of instabilities in two parallel-connected boost converters under current mode control," in *Power Electronics and Applications, 2005 European Conference on*, 2005, p. 8 pp.
- [9] S. K. Mazumder, "Stability analysis of parallel DC-DC converters," *Aerospace and Electronic Systems, IEEE Transactions on*, vol. 42, pp. 50-69, 2006.
- [10] J. M. Zhang, X. G. Xie, X. K. Wu, and Q. Zhaoming, "Stability study for paralleled DC/DC converters," in *Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual*, 2004, pp. 1569-1575 Vol.2.
- [11] C. Wm.T.Mclyman, *Transformer and Inductor Design Handbook, Third Edition*. New York: Routledge, 2004.
- [12] P. Wallmeier, "Pre-optimization of linear and nonlinear inductors using area-product formulation," in *Industry Applications Conference, 2002. 37th IAS Annual Meeting. Conference Record of the*, 2002, pp. 2445-2450 vol.4.

A.3 Boost Converter with Three-Stage Switching Cell and Integrated Magnetics (APEC 2009)

Boost Converter with Three-State Switching Cell and Integrated Magnetics

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Abstract – Fuel cell systems often require high voltage gain and dc-dc step-up converter is a critical part. Scope of this paper is integration of inductor and transformer on a single core. Usage of integrated magnetics improves utilization of magnetic core and thus size and weight of the converter may be reduced.

I. INTRODUCTION

An increasing interest in alternative and renewable energy creates a demand for novel power conversion systems, which interfaces different energy source to a load or to a utility grid. Very often it's necessary to boost a low voltage from a source (small fuel cells, most of photovoltaic panels) to a high voltage suitable for an inverter. The required voltage gain may exceed value of 20 in many cases. Such gain is attainable for boost converter with SiC diodes and CoolMOS transistors, but by a cost of poor semiconductors utilization and limited efficiency [1]. In the literature [2-6] one may find several topologies with a coupled inductor, which offer a high voltage gain. The main drawback among these topologies is large input current ripple and such ripples may lead to PV maximum power point tracking mismatch or to quick degradation of a fuel cell. For these reasons an additional input filter is required, but it increases size, cost and complexity of the converter. The topology introduced in [7] and presented on Fig. 1 offers a high voltage gain, reduced voltage rating of MOSFETs and input current ripple is limited by inductor L_M . Reference [8] reports a very good performance of this topology in a high voltage gain application, like a fuel cell. However in such application the converter has to operate under variable, load dependent input voltage. Typically for fuel cell minimum to maximum input voltage ratio is about 1:2 [9]. While the converter operates under different conditions it might be difficult to optimize magnetic components. On one hand they are sized for high input current. On the other hand they are designed for the highest input voltage too. But in fuel cell application high voltage and high current doesn't occur at the same time. It may result in poor utilization of magnetic cores of the inductor and the transformer.

The main focus in this paper is to design and implement of an integrated magnetic, which should reduce size and weight of the converter.

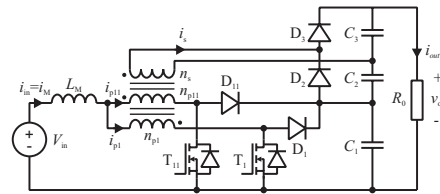


Fig. 1 - Diagram of a boost converter with a three state switching cell and a voltage multiplier

II. ANALYSIS OF THE CONVERTER

The selected topology is presented on Fig. 1. It incorporates so called 3-state switching cell (T_1 , T_{11} , D_1 , D_{11} and the transformer) [7, 10]. Explanation of the converter's operation maybe more intuitive if one considers this topology as a modified current fed push-pull converter – with diodes D_1 , D_{11} and capacitor C_1 as a lossless clamp for transistors.

Key waveforms are presented on Fig. 2. Basically the converter operates with transistor duty cycle larger than 50 %, i.e. overlapping mode. Assuming continuous conduction mode (CCM) there are four operating modes. Mode 1 and 3 are identical while both transistors are turned-on and share the current equally ($n_{p1}=n_{p11}$). During this period input inductor

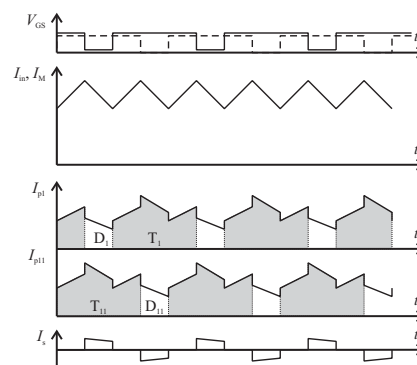


Fig. 2 - Main waveforms of the converter

L_M is being charged. Because both primary windings are shorted there is no voltage across secondary winding, so there is no current flow in the secondary winding too. Next, in mode 2 transistor T_1 is being turned-off and energy stored in L_M is being released thru primary winding (n_{p1}) and diode D_1 to capacitor C_1 , and thru secondary winding and diode D_3 to capacitor C_3 . The last mode 4 is symmetrical to mode 2 – while transistor T_1 remains turned-on and T_{11} is turned-off. During this period diode D_{11} and diode D_2 conduct. Capacitors C_1 and C_2 are recharged.

It's important that capacitor C_1 is recharged twice during the switching period, while capacitors C_2 and C_3 are recharged only once. Static voltage gain of the converter is given by (1), where n is primary to secondary turns ratio. Voltage stress is given by (2) for primary side semiconductors and by (3) for secondary side diodes D_2 and D_3 .

$$V_{out} = V_{in} \cdot \frac{1+n}{1-D} \quad (1)$$

$$V_{T1} = V_{T11} = V_{D1} = V_{D11} = V_{out} \cdot \frac{1}{1+n} \quad (2)$$

$$V_{D2} = V_{D3} = V_{out} \cdot \frac{n}{n+1} \quad (3)$$

III. MAGNETIC COMPONENTS

Magnetic components are essential for any dc-dc converter design. Their performance reflects directly on converter's performance. So, typical design of magnetics focuses on reduction of losses inside magnetics and on reduction of parasitics, so external circuit is not affected. But on the other hand the magnetics are significant part of the converter size and weight, so size reduction should be taken into consideration too. In many cases integration of magnetics may improve utilization of a core and thus size may be reduced.

A. Dc inductor

In considered topology dc inductor L_M conducts essentially

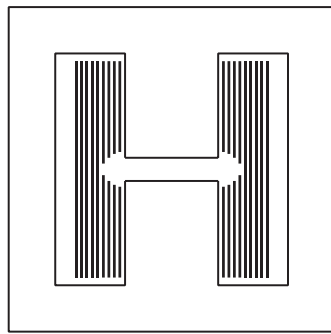


Fig. 3 - Notched foil winding with low dc and ac resistance arranged on EE ferrite core

dc current with relatively small ac component (ripples). Majority of dc current content allows using of a round wire for inductor winding. It characterizes relatively low cost and good copper fill factor K_u . Since dc current is dominant a low dc resistance is a key. In order to improve copper fill factor one may use two or three thinner wires instead of thick single wire. But this approach makes the winding more complex and expensive. If required number of turns is relatively small one may incorporate a foil winding, which provides excellent copper fill factor. There are two main drawbacks of an inductor foil windings, especially when ac current component increases. First, it's a multilayer design and one turn means one layer so proximity losses become significant very quickly. The solution is a design with as few turns as possible. Second significant drawback relates to an air gap in a ferrite core. Because of a fringing field huge eddy currents induces in inner layers of the winding. It creates significant losses and risk of hot spot. Using of a distributed air gap or a powder core helps to solve this problem. If a gapped ferrite core is the only option then special winding arrangement is necessary. It's simply done by notching inner layers around the air gap, so fringing field doesn't penetrate the winding [11, 12]. Example of such winding is shown on Fig. 3.

A design procedure based on area-product approach is well described in [13], so here only few most important steps are presented. First, required inductance L_M is to be determined and for considered converter it's given by (4), where ΔI_M is amplitude of current ripples. By rearranging (4) it's found that the largest current ripples occur at duty cycle $D=0.75$.

$$L_M = \frac{V_{out} \cdot (D-0.5) \cdot (1-D)}{f_s \cdot 2 \cdot \Delta I_M \cdot (1+n)} \quad (4)$$

Assuming that the inductor operates in linear region, below saturation it's easy to find dc and ac induction components (B_{ind} and ΔB_{ind}) while they are directly proportional to inductor current dc and ac components ($I_{M(dc)}$ and ΔI_M).

Core size is characterized by area product A_p , which is product of core cross section area A_c and window area W_a [13]. Required area product value is given by (5). Current $I_{M(dc)}$ is maximum inductor dc current, i.e. at minimum input voltage and rated power. When the dimensions of the core are known one may find required number of turns (6) and length of the air gap (7).

$$A_p = \frac{L_M \cdot I_{M(dc)} \cdot (I_{M(dc)} + \Delta I_M)}{(B_{ind} + \Delta B_{ind}) \cdot J \cdot K_u} \quad (5)$$

$$n_M = \frac{L_M \cdot \Delta I_M}{\Delta B_{ind} \cdot A_c} \quad (6)$$

$$l_g = \frac{\mu_0 \cdot n_M^2 \cdot A_c}{L_M} \quad (7)$$

For small air gaps effective area of the gap A_g is close to core cross section area A_c , but larger gaps effective area of the gap is larger and have to be corrected [13].

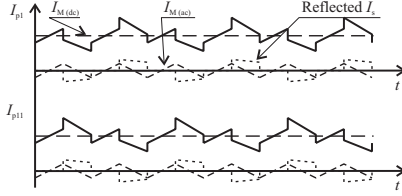


Fig. 4 - Primary currents and its components

B. Transformer

Fig. 4 presents primary currents and its components: input dc current, input current ripples and reflected secondary current. This combination of ac and dc components creates challenge for design of transformer windings. Reduction of both, dc and ac resistances of primary windings, is crucial. Usage of Litz wire helps to reduce skin and proximity effects. Unfortunately in the same time Litz wire has poor copper fill factor K_u , so dc resistance of such winding is high. Also leakage inductance of such winding is high affecting the external circuit. Round wire has better copper fill factor and dc resistance is reduced in compare to Litz wire. But due to skin effect ac loss is fairly high.

Foil winding seems to be a good solution. It has a very good copper fill factor and resulting dc resistance is low. Small thickness of the foil reduces skin effect, while interleaving of primary and secondary windings attenuates proximity effect [14].

Design procedure based on area product A_p is described in details in [13]. First, size of the core is calculated from (8). Variable P_t is transformer apparent power, i.e. sum of input and output power of the transformer. For push-pull transformer it's given by (9).

$$A_p = \frac{P_t}{2 \cdot K_u \cdot K_f \cdot \Delta B_{tr} \cdot J \cdot f_s} \quad (8)$$

$$P_t = 1.41 \cdot P_{in} + P_{out} \quad (9)$$

Induction amplitude ΔB_{tr} may not exceed saturation level of the core. However in many cases peak induction in the transformer is well below saturation because of maximum allowed core losses. Specific core loss P_{fe} as a function of induction amplitude and switching frequency is given by well known Steinmetz equation (10). In considered converter primary winding number of turns is given by (11), which is true for $D=(0.5, 1)$.

$$P_{fe} = k \cdot f_s^\alpha \cdot \Delta B_{tr}^\beta \quad (10)$$

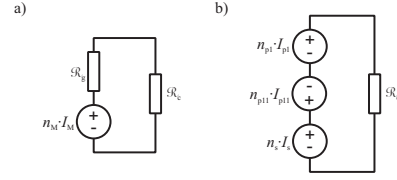


Fig. 5 - Magnetic circuits of an inductor (a) and a push-pull transformer (b)

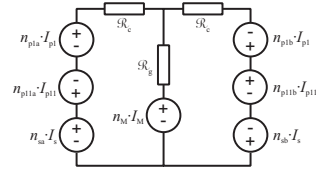


Fig. 6 - Magnetic circuit of the integrated inductor-transformer

$$n_{p1} = n_{p11} = \frac{1}{2 \cdot \Delta B_{tr} \cdot A_c} \cdot \frac{V_{out}}{2 \cdot (1+n)} \cdot \frac{1-D}{f_s} \quad (11)$$

It's found that the largest induction amplitude occurs at duty cycle $D=0.5$, i.e. for the highest input voltage.

C. Integrated magnetics

Fig. 5a presents magnetic circuits of an inductor. Magneto-motive force (MMF) is represented as voltage source $n_M \cdot I_M$, while the air gap reluctance is represented by linear resistor R_g . Resistor R_c represents reluctance of the ferrite core and it's very small in compare to reluctance of the air gap ($R_c \ll R_g$).

Fig. 5b shows magnetic circuit of a push-pull transformer. There are three voltage sources representing MMF of windings. MMFs directions refer to the converter diagram on Fig. 1. Reluctance of the core is represented by resistor R_c .

These two circuits can be combined together on a single EE core. The simplest way is to place the inductor winding on the center gapped leg. Resulting magnetic circuit is shown on Fig. 6. Transformer windings are split into two identical halves and placed on outer legs. In this way flux generated by inductor winding does not affect transformer windings. Also flux generated by the transformer has no influence on the inductor. Unfortunately it results in complex winding arrangement, large overall number of turns and large winding resistance.

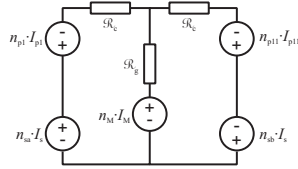


Fig. 7 - Reduced magnetic circuit of the integrated inductor-transformer

Analyzing primary side current waveforms presented on Fig. 4 one may find that input current flows thru transformer primary windings. Since there is agreement between current waveforms it's possible to use transformer primary windings as a part of the inductor winding. For proper operation of the transformer the secondary winding is split and arranged on both outer legs, so it's not affected by inductor flux. Proposed magnetic circuit is presented on Fig. 7 and currents directions refers to Fig. 1. The magnetic circuit from Fig. 7 is described by (12), where L_M is self inductance of n_M winding, M_{Mp1} is mutual inductance between n_M and n_{p1} windings and so on.

Design of the integrated magnetic is an iterative process. When both transistors are turned-on the input voltage is applied to inductor and transformer's primary windings, so (13) is truth. Assuming that secondary current i_s is zero and both primary currents are equal $i_{p1}=i_{p11}$ one can write (14) and (15). Combining these equations with (13) gives equivalent inductance L_{Meq} (16). With good coupling between both primary windings mutual inductance M_{p1p11} value is close to self inductance L_{p1} value, so they will cancel each other. Equivalent inductance L_{Meq} is larger then physical inductance L_M , so in this way required inductance L_M is reduced.

$$\begin{bmatrix} v_M \\ v_{p1} \\ v_{p11} \\ v_{sa} \\ v_{sb} \end{bmatrix} = \begin{bmatrix} L_M & M_{Mp1} & M_{Mp11} & -M_{Msa} & -M_{Msb} \\ M_{p1M} & L_{p1} & -M_{p1p11} & -M_{p1sa} & -M_{p1sb} \\ M_{p11M} & -M_{p11p1} & L_{p11} & M_{p11sa} & M_{p11sb} \\ -M_{saM} & -M_{sap1} & M_{sap11} & L_{sa} & M_{sasb} \\ M_{sbM} & -M_{sbp1} & M_{sbp11} & M_{sbbsa} & L_{sb} \end{bmatrix} \cdot \begin{bmatrix} \frac{di_M}{dt} \\ \frac{di_{p1}}{dt} \\ \frac{di_{p11}}{dt} \\ \frac{di_{sa}}{dt} \\ \frac{di_{sb}}{dt} \end{bmatrix} \quad (12)$$

$$V_{in} = v_M + v_{p1} = L_{Meq} \cdot \frac{di_M}{dt} \quad (13)$$

$$v_M = L_M \cdot \frac{di_M}{dt} + M_{Mp1} \cdot \frac{di_{p1}}{dt} + M_{Mp11} \cdot \frac{di_{p11}}{dt} \quad (14)$$

$$v_{p1} = M_{p1M} \cdot \frac{di_M}{dt} + L_{p1} \cdot \frac{di_{p1}}{dt} - M_{p1p11} \cdot \frac{di_{p11}}{dt} \quad (15)$$

$$L_{Meq} = L_M + M_{Mp1} + M_{Mp11} + \frac{1}{2} \cdot L_{p1} - \frac{1}{2} \cdot M_{p1p11} \quad (16)$$

Approximated core size is found using area product approach simply by summarizing area product required by the

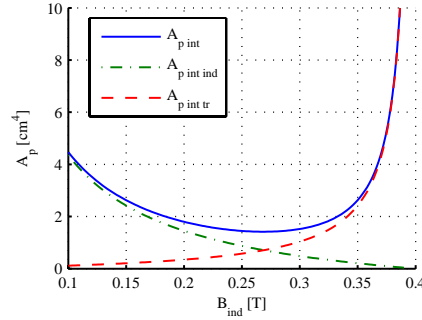


Fig. 8 - Integrated inductor-transformer required area product versus inductor flux

transformer and by the inductor (17). One can change ratio between the inductor and the transformer flux and find minimum required core size. Fig. 8 presents how required area product depends on inductor flux. This method gives only approximated core size, but it's a good starting point for further optimization.

$$A_p = \frac{P_t}{2 \cdot K_u \cdot K_f \cdot \Delta B_{tr} \cdot J \cdot f_s} + \frac{L_{Meq} \cdot I_{M(dc)} \cdot (I_{M(dc)} + \Delta I_M)}{(B_{ind} + \Delta B_{ind}) \cdot J \cdot K_u} \quad (17)$$

Once the core size is determined inductor and transformer windings are designed according to guidelines presented in previous sections. First, number of turns in transformer winding is found with (11). Next, in an iterative process one can find self inductances and mutual inductances (12), find required number of turns n_M (6) and size of the air gap l_g (7).

Contrary to typical transformer, the integrated magnetic usually operates under significant dc flux conditions. It has two major effects. First, because of dc flux in the core increased core losses may occur. Unfortunately core datasheets contain power loss data only for pure sinusoidal excitation, so it's difficult to calculate core losses in advance. Second, the peak induction is higher in compare to traditional transformer. Thus there is no space for any undesired dc flux. It requires careful control of dc current flowing in primary windings n_{p1} and n_{p11} .

IV. EXPERIMENTAL SETUP AND RESULTS

In order to verify theoretical analysis and calculations a 300 W breadboard is built and tested. Input voltage varies from 30 to 50 Vdc and output voltage is regulated at 400 Vdc. Switching frequency is $f_s=50$ kHz and the transformer turns ratio is $n=2$. According to (2) it allows using 150 V MOSFETs (IRFP4321PbF) and 150 V Schottky diodes (30CPQ150PbF) on primary side. On the secondary side of the transformer there are 600 V SiC diodes (IDT10S60C).

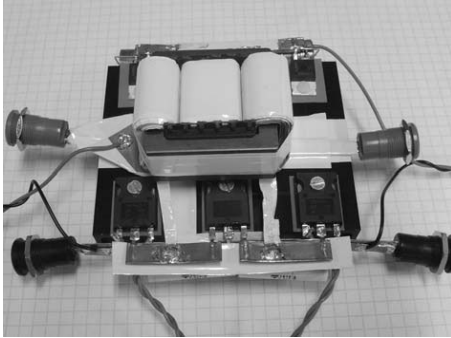
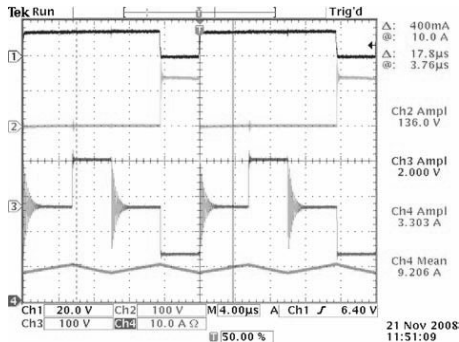


Fig. 9 - Assembled converter with integrated inductor-transformer

Fig. 10 - Main waveforms of the converter
Ch1 - gating signal; Ch2 - V_{DS} ; Ch3 - V_{n2} ; Ch4 - I_{in}

It's found that E42/21 core (0P44022EC) is sufficiently large. With $n_M=7$ turns and 1 mm air gap in the center leg it gives inductance $L_M=16\mu H$. Transformer induction amplitude is limited to $\Delta B_{tr}=0.15$ T at the highest input voltage and it's limited by core losses. Transformer primary winding has $n_{p1}=n_{p11}=12$ turns, which results in equivalent inductance $L_{Meq}=46\mu H$. The secondary winding has $n_s=24$ turns and it's divided into two halves, $n_{sa}=n_{sb}=12$ turns on each of outer legs. Primary and secondary windings are interleaved to reduce proximity effect and ac losses. Assembled 300 W breadboard is presented on Fig. 9. Fig. 10 presents basic operational waveforms of the converter at 30 V input voltage.

Control of primary windings dc currents is critical to avoid outer legs saturation. In case of integrated inductor-transformer it's possible to detect such saturation by observation of the input current only. Fig. 11 shows the input current and its spectrum in an unsaturated and balanced case. The input current has only a large dc component and 100 kHz component, which refers to ripples at double switching frequency. In case of small unbalance of transformer primary currents one of outer legs become saturated and shape of the

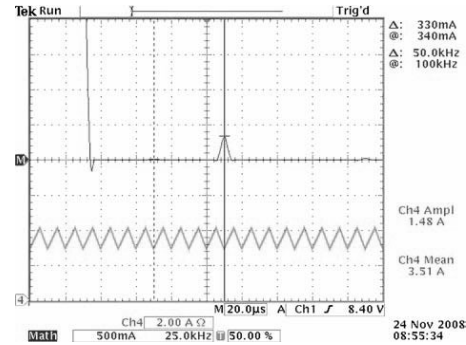
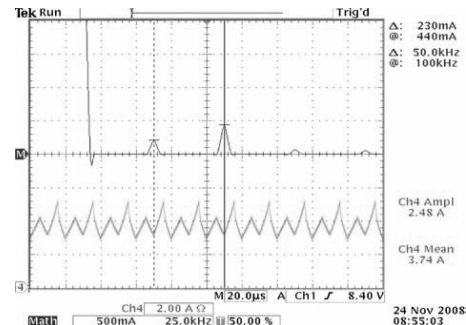
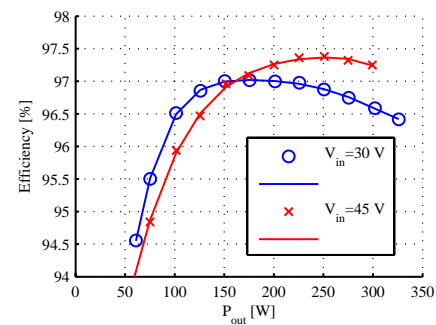
Fig. 11 - Input current I_{in} (bottom) and its spectrum (top) in balanced caseFig. 12 - Input current I_{in} (bottom) and its spectrum (top) in unbalanced, saturated case

Fig. 13 - Measured efficiency of the converter

input current changes. Now, 50 kHz component appears in the current spectrum presented on Fig. 12.

Fig. 13 presents measured efficiency of the converter at 30 V and 45 V input voltage. For lower input voltage efficiency

peaks at 97% at 175 W and remains above 96.5% up to 300 W. For higher input voltage efficiency exceeds 97%.

V. CONCLUSION

A boost converter with a three state switching cell and integrated magnetic has been presented in this paper. The converter has the inductor and the push-pull transformer arranged on a standard gapped EE core. Such integration allows using of transformer primary windings as a part of the inductor winding, thus smaller physical inductance is required. It results in smaller and lighter core. To verify the idea 300 W breadboard is built and tested. The breadboard exhibits good performance. Also size of the magnetic components is reduced.

ACKNOWLEDGEMENT

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REFERENCES

- [1] P. Klimczak and S. Munk-Nielsen, "Comparative study on paralleled vs. scaled dc-dc converters in high voltage gain applications," in *Power Electronics and Motion Control Conference, 2008. EPE-PEMC 2008. 13th*, 2008, pp. 108-113.
- [2] B. Ju-Won, R. Myung-Hyo, K. Tae-Jin, Y. Dong-Wook, and K. Jong-Soo, "High boost converter using voltage multiplier," in *Industrial Electronics Society, 2005. IECON 2005. 31st Annual Conference of IEEE*, 2005, p. 6 pp.
- [3] Z. Qun and F. C. Lee, "High-efficiency, high step-up DC-DC converters," *Power Electronics, IEEE Transactions on*, vol. 18, pp. 65-73, 2003.
- [4] W. Rong-Jong and D. Rou-Yong, "High step-up converter with coupled-inductor," *Power Electronics, IEEE Transactions on*, vol. 20, pp. 1025-1035, 2005.
- [5] K. C. Tseng and T. J. Liang, "Novel high-efficiency step-up converter," *Electric Power Applications, IEE Proceedings -*, vol. 151, pp. 182-190, 2004.
- [6] R. J. Wai and R. Y. Duan, "High-efficiency DC/DC converter with high voltage gain," *Electric Power Applications, IEE Proceedings -*, vol. 152, pp. 793-802, 2005.
- [7] G. V. Torrico-Bascope, R. P. Torrico-Bascope, D. S. Oliveira, F. L. M. Antunes, S. V. Araujo, and C. G. C. Branco, "A Generalized High Voltage Gain Boost Converter Based on Three-State Switching Cell," in *The 32nd Annual Conference of the IEEE Industrial Electronics Society IECON'06*, Paris, France, 2006, pp. 1927-1932.
- [8] P. Zacharias, B. Sahan, S. V. Araújo, F. L. M. Antunes, and R. T. Bascopé, "Analysis and Proposition of a PV Module Integrated Converter with High Voltage Gain Capability in a non-isolated Topology," in *The 7th International Conference on Power Electronics Daegu, Korea: IEEE*, 2007.
- [9] W. Vielstich, *Handbook of fuel cells fundamentals, technology, and applications* editors, Wolf Vielstich, Arnold Lamm, Hubert A. Gasteiger: Wiley, 2003.
- [10] G. V. T. Bascope and I. Barbi, "Generation of a family of non-isolated DC-DC PWM converters using new three-state switching cells," in *Power Electronics Specialists Conference, 2000. PESC 00. 2000 IEEE 31st Annual*, 2000, pp. 858-863 vol.2.
- [11] J. D. Pollock and C. R. Sullivan, "Gapped-inductor foil windings with low AC and DC resistance," in *Industry Applications Conference, 2004. 39th IAS Annual Meeting. Conference Record of the 2004 IEEE*, 2004, p. 557.
- [12] J. D. Pollock and C. R. Sullivan, "Modelling Foil Winding Configurations with Low AC and DC Resistance," in *Power Electronics Specialists Conference, 2005. PESC '05. IEEE 36th*, 2005, pp. 1507-1512.
- [13] C. W. T. McLyman, *Transformer and inductor design handbook*: Marcel Dekker, 2004.
- [14] M. Nyman and M. A. E. Andersen, "A new approach to high efficiency in isolated boost converters for high-power low-voltage fuel cell applications," in *Power Electronics and Motion Control Conference, 2008. EPE-PEMC 2008. 13th*, 2008, pp. 127-131.
- [15] S. Cuk, "New magnetic structures for switching converters," *Magnetics, IEEE Transactions on*, vol. 19, pp. 75-83, 1983.

A.4 High Efficiency Boost Converter with Three State Switching Cell (PCIM 2009)

High Efficiency Boost Converter with Three State Switching Cell

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Abstract

The boost converter with the three-state switching cell seems to be a good candidate for a dc-dc stage for non-isolated generators based on alternative energy sources. It provides a high voltage gain, a reduced voltage stress on transistors and limited input current ripples. In this paper the focus is on performance improvement of this type of the converter. Use of foil windings helps to reduce conduction losses in magnetic components and to reduce size of these components. Also it has been demonstrated that the regulation range of this type of converter can be increased by operation with duty cycle lower than 50%.

1. Introduction

Increasing interest in alternative and renewable energy creates a demand for novel power conversion systems, which interfaces different energy sources to a load or to an utility grid. Very often it's necessary to boost a low voltage from a source (commercial fuel cells, most of photovoltaic panels) to a high dc voltage suitable for an inverter. In many cases safety isolation is not required, thus it's possible to use a non-isolated topology. The required voltage gain may exceed value of 20 in some cases. Such gain is attainable for a basic boost converter with SiC diodes and novel MOSFET transistors (SuperFET, CoolMOS etc.), but by a cost of poor semiconductor utilization and the efficiency limited by MOSFET conduction losses [1]. Further efficiency improvement requires low voltage switches which ensure lower conduction losses and improved switching performance. In the literature [2-6] one may find several topologies based on a coupled inductor principle, which offer a high voltage gain and reduced voltage stress on the active switch. The main drawback among these topologies is large input current ripples. On one hand significant input current ripples may lead to faster degradation of a fuel cell stack or disturb maximum power point tracking in case of PV application. An additional input filter can solve these problems, but it increases size, complexity and cost of the converter. Also large ripples result in a large peak current, which leads to increased conduction losses and requires oversized components. The topology introduced in [7] and presented on Fig. 1 offers a high voltage gain and reduced voltage stress on transistors. Reference [8] reports a very

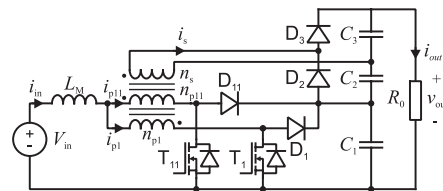


Fig. 1. Diagram of the three state switching cell boost converter

good performance of this topology in high voltage gain application ($V_{in}=35\text{ V}$, $V_{out}=400\text{ V}$). The main focus of this paper is to improve a power density and an efficiency of this type of converter.

2. Description of the converter

The selected topology is presented on Fig. 1. It incorporates so called three-state switching cell

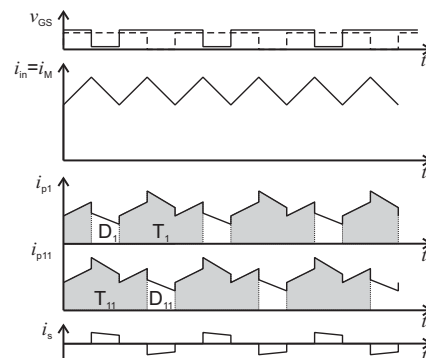


Fig. 2. Basic waveforms of the converter

(switches T_1 , T_{11} , D_1 , D_{11} and the transformer) [7, 9]. The secondary side of the transformer with diodes D_2 , D_3 and capacitors C_2 , C_3 compose the voltage doubler rectifier. Basically the converter operates in so called overlapping mode, i.e. with the duty cycle larger than 50% and in continuous conduction mode (CCM).

2.1. Operation with duty cycle larger than 50%

Key waveforms for are presented on Fig. 2. There are four basic operating modes. Mode 1 and 3 are identical while both transistors are turned-on and share the input current equally ($n_{p1}=n_{p11}$). During this period the input inductor L_M is being charged. Both primary windings are effectively connected anti-parallel. In this case no voltage induces in the secondary winding and there is no current flow in the secondary winding too. Next, in mode 2 the transistor T_1 is being turned-off and energy stored in L_M is being released thru the primary winding (n_{p1}) and the diode D_1 to the capacitor C_1 , and thru the secondary winding and the diode D_3 to the capacitor C_3 . In this operating mode primary windings are effectively connected in series and the voltage V_{C1} is applied to them. The voltage equal to $V_{C1} \cdot n$ induces in the secondary winding. Term n means the transformer primary-to-secondary turns ratio. The last mode 4 is similar to mode 2 – while transistor T_1 remains turned-on and T_{11} is turned-off. In this mode diodes D_{11} and D_2 conduct. It's important that the capacitor C_1 is charged twice over one cycle, while capacitors C_2 and C_3 are charged only once. The converter voltage gain in CCM is given by (1). The maximum voltage across switches is given by (2) and (3).

$$V_{out} = \frac{1+n}{1-D} \cdot V_{in} \quad (1)$$

$$V_{T1max} = V_{D1max} = V_{C1} = \frac{1}{1+n} \cdot V_{out} \quad (2)$$

$$V_{D2max} = V_{D3max} = \frac{n}{1+n} \cdot V_{out} \quad (3)$$

2.2. Operation with duty cycle lower than 50%

Unlike a conventional current-fed push-pull converter [10] the topology presented on Fig. 1 is able to operate with the duty cycle lower than 50%. However the voltage gain function becomes strongly non-linear in this case. For duty cycles just below 50% converter operates normally and it's voltage gain follows (1). Also the voltage stress on components fits to (2) and (3). On the other

end, at the very low duty cycles the converter behaves like a two-phase interleaved boost with coupled inductor [11]. In this case voltage gain is given by (4).

$$V_{out} = \frac{1}{1-2 \cdot D} \cdot V_{in} \quad (4)$$

Under such conditions diodes D_2 and D_3 are forward biased all the time so there is no voltage across capacitors C_2 and C_3 . The whole the output voltage appears across the capacitor C_1 . It may create an additional voltage stress on transistors and diodes D_1 and D_{11} .

The boundary between one and the other mode is defined by the crossing of voltage gain functions (1) and (4). By combining these two equations one may find the critical duty cycle D_{cr} at the crossing point (5).

$$D_{cr} = \frac{n}{2 \cdot n + 1} \quad (5)$$

3. Magnetic components

Magnetic components are essential for any dc-dc converter design. Their performance reflects directly on converter's performance. Typically design and optimization process focuses on loss reduction inside magnetics as well as on reduction of parasitics, so external circuit is not affected. Volume of magnetics is an important issue too.

3.1. Dc inductor

In the considered topology the dc inductor L_M conducts essentially the dc current with limited ac component (ripples). It means that the flux ac component is fairly low too, thus core losses are small and the design is so called saturation limited design [12]. To improve performance of such design it is important to reduce dc and ac

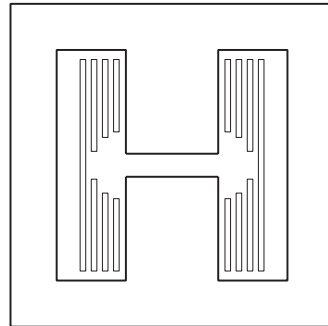


Fig. 3. Foil winding arrangement on a gapped core

conduction losses, but low dc resistance is crucial. Basically one may choose between a solid round wire, a Litz wire and a foil winding. Use of a single round wire provides a good window fill factor, a low dc resistance and a low manufacturing cost. To improve window utilization one may use few thinner wires or a rectangular wire if available. Another choice is a Litz wire which provides a good ac/dc resistance ratio, but it requires a larger window area because of a poor copper fill factor. Finally a winding made of a copper foil may provide a very good copper fill factor (depends on copper and insulation thickness) and a very low dc resistance. However two main drawbacks are recognized. First, it's a multilayer design since one turn means one layer. In this case proximity losses may become large quickly. The solution is to use as few turns as possible and the copper thickness smaller than the penetration depth for given frequency. Second drawback relates to use of a ferrite core with a discrete air gap. Because of a fringing field around the air gap huge eddy currents induce in inner layers of the winding. It creates large losses and risk of hot spot in proximity of the gap. This issue is solved by use of a core with distributed air gap, e.g. a powder core. If a core with a discrete air gap is an only option then the special winding arrangement is necessary. It is simply done by notching of inner layers of the winding, so the fringing field doesn't penetrate thru the winding [13, 14]. An example of such winding is presented on Fig. 3.

3.2. Three winding transformer

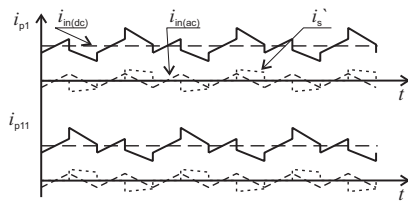


Fig. 4. Transformer primary currents and their components

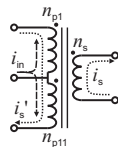


Fig. 5. Primary currents flow in transformer windings

Fig. 4 presents transformer primary currents and its components: the input dc current $i_{in(dc)}$, the input current ripple $i_{in(ac)}$ and the reflected secondary current i_s' . Fig. 5 shows how these components flow in particular windings of the transformer. The input current flows into the beginning of the winding n_{p11} and into the end of the winding n_{p1} like presented on Fig. 1 and Fig. 5. For this current component primary windings are effectively connected anti-parallel. In an ideal case half of the input current flows into one primary winding while the other half goes into the other. In this way fluxes generated by these currents cancel each other, so there is no effect on the secondary side of the transformer. Secondary current i_s flows in the secondary winding and the reflected secondary current i_s' flows in primaries as presented on Fig. 5. For this current component primary windings are connected effectively in series.

Such mixture of ac and dc components creates a challenge for the design of transformer windings, especially primaries. Reduction of dc and ac resistances of primary windings is crucial. Use of a Litz wire helps to reduce skin and proximity effects and provides a good ac/dc resistance ratio. Unfortunately in the same time a Litz wire has a poor copper fill factor, and thus requires a core with a large window. Also the leakage inductance of such winding is high. A round wire has a better copper fill factor and a dc resistance is reduced in compare to the Litz wire. But due to the skin effect the ac loss is fairly high. By taking several thinner round wires one may reduce layer thickness and the ac resistance, but it requires fairly complicated winding arrangement. A foil winding seems to be a good solution once again. It has a very good copper fill factor and the dc resistance is low. Small thickness of the foil reduces the skin effect, while interleaving of primary and secondary

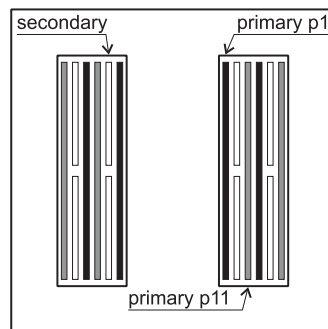


Fig. 6. A three winding transformer foil windings arrangement

windings attenuates the proximity effect [15].

The proposed winding arrangement of the three winding transformer is presented on Fig. 6. Primary and secondary windings are interleaved. Primary windings n_{p1} and n_{p11} are made of a thin foil occupying whole available window width. Each of primary windings has just a single turn per layer and the secondary winding is sandwiched between primaries. The secondary winding has few turns arranged in a single layer like presented on Fig. 6. Such winding arrangement provides low dc and ac resistances for all mentioned above current components and a good coupling between primary and secondary windings. This solution has two main drawbacks. First, because of intensive interleaving there is a large surface area of primary and secondary winding facing each other. Depends on the insulation material and the insulation thickness it may result in a significant interwinding capacitance which decreases performance. The second drawback is reduced flexibility in terms of turns ratio. It's fairly easy to achieve integer turns ratio, like 1:2 or 1:3. But it may be difficult to achieve non-integer turns ratio, like 1:2.5.

4. Experimental results

In order to verify theoretical analysis and simulations the 500 W breadboard has been built and tested. The converter input voltage is 30-50 V and the output voltage is regulated at 400 V. The switching frequency is $f_s=50$ kHz. The assembled converter is presented on Fig. 7. The inductor L_M bases on E42/21 ferrite core with 1 mm air gap. The winding is made of 24x0.3 mm copper foil and there are 12 turns, which gives the inductance $L_M=47$ μ H. It limits input current ripples to 3.5 A peak to peak, which is about 20% of the maximum input dc current. Measured dc resistance of the inductor winding is $R_{Mdc}=2.7$ m Ω while respective ac resistance is $R_{Mac}=120$ m Ω for 100 kHz (double

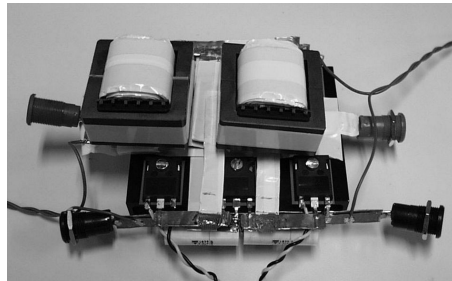


Fig. 7. Assembled 500 W converter

of the switching frequency). The transformer bases on E42/21 core too. Because of core losses its peak induction is limited to 0.15 T at high input voltage and it requires at least 6 turns in each of primary windings. Primary windings are made of 24x0.15 mm copper foil. The transformer turns ratio is $n_{p1}:n_{p11}:n_s=1:1:2$, thus the secondary winding has 12 turns and it's made of 10x0.15 mm copper foil. Measured dc resistance is $R_{p1dc}=R_{p11dc}=3$ m Ω for the primary winding and $R_{sdc}=12$ m Ω for the secondary. The ac resistance of the transformer is measured in respect to particular current components flowing in its windings and described in section 3.2. The ac resistance seen from the secondary winding while primaries are connected in series and shorted is $R_{sac}+R_{p1ac}+R_{p11ac}=21$ m Ω . This resistance is related to the secondary current and the reflected secondary current. Next the resistance for input current dc and ac components is evaluated with primary windings connected anti-parallel.

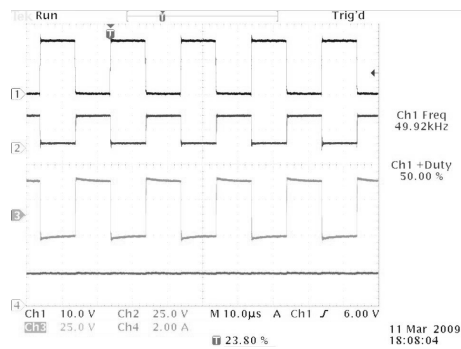


Fig. 8. Waveforms of the converter operating with $V_{in}=10$ V and 50% duty cycle

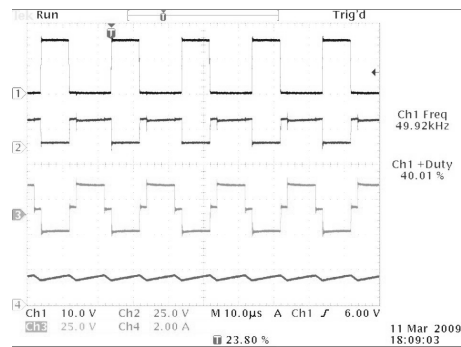


Fig. 9. Waveforms of the converter operating with $V_{in}=10$ V and 40% duty cycle

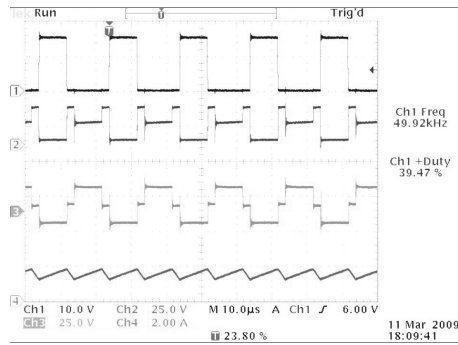


Fig. 10. Waveforms of the converter operating with $V_{in}=10V$ and 39.5% duty cycle

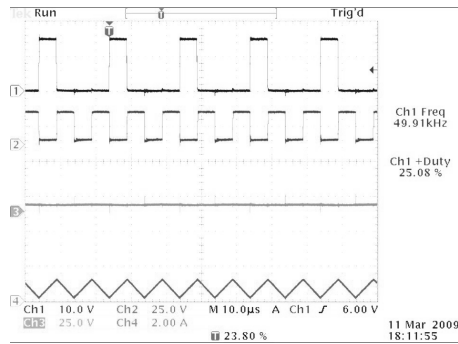


Fig. 11. Waveforms of the converter operating with $V_{in}=10V$ and 25% duty cycle

Measured dc resistance is about $R_{p1dc}||R_{p1dc}=1.5$ m Ω and the ac resistance is about $R_{p1ac}||R_{p1ac}=1.8$ m Ω . The transformer turns ratio is 1:1:2 and it enables to use of 150 V MOSFETs (IRF4321PbF). Diodes D_1 and D_{11} are 150 V Schottky's (30CPQ150PbF) while D_2 and D_3 are 600 V SiC diodes (IDT10S60C).

Next, the test at low duty cycles and reduced input voltage is being performed. The input voltage is set to 10 V and the duty cycle is changed from 50% down to 25%. From (5) it's found that the critical duty cycle $D_{cr}=40\%$. Fig. 8, Fig. 9, Fig. 10 and Fig. 11 present observed waveforms at 50%, 40%, 39.5% and 25% duty cycle respectively. On these figures Ch1 presents the gating signal for the transistor, Ch2 presents the drain-source voltage of the respective transistor, Ch3 presents the transformer secondary voltage and Ch4 presents the input current. The voltage V_{C1} is determined by the transistor drain-source peak voltage (Ch2),

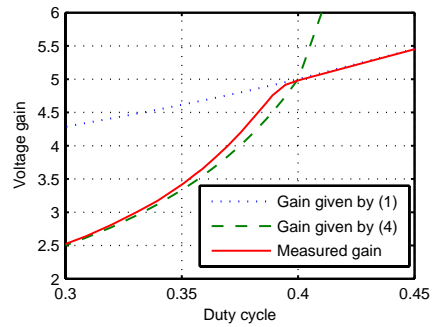


Fig. 12. Voltage gain of the converter operating at low duty cycle

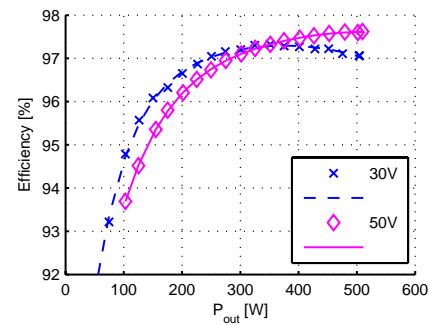


Fig. 13. Measured efficiency of the converter for 30 V and 50 V input voltage

while voltages V_{C2} and V_{C3} are given by the transformer secondary voltage (Ch3). For duty cycles 50% and 40% output capacitors share the output voltage equally and the voltage gain follows (1). When the duty cycle decreases just below D_{cr} (Fig. 10) the voltage V_{C1} quickly increases (the peak of Ch2) and voltages V_{C2} and V_{C3} decrease (the amplitude of Ch3). When the duty cycle decreases farther then the transformer secondary voltage collapses down to zero. In this case only the capacitor C_1 contributes to the output voltage. Fig. 12 compares theoretical voltage gains (given by (1) and (4)) against measured voltage gain. Finally the efficiency of the converter has been measured using four precision digital multimeters Fluke 8845A. Since the input current exceeds the multimeter current range an external precise shunt resistor has been used. Measured efficiency curves are presented on Fig. 13.

5. Conclusion

This paper describes the boost converter with the three-state switching cell. To improve the design and reduce size of the converter foil windings are used instead of round wires or Litz wires. The dc inductor with foil winding is characterized by a very low dc resistance. For the three winding transformer (the push-pull transformer) proper arrangement of foil windings ensures a very low resistance for all current components present in its windings. Measured peak efficiency exceeds 97% for low and high input voltage. Also it has been demonstrated that the regulation range of this type of converter can be increased by operation with duty cycle between 50% and D_{cr} .

Acknowledge

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References

- [1] P. Klimczak and S. Munk-Nielsen, "Comparative study on paralleled vs. scaled dc-dc converters in high voltage gain applications," in *Power Electronics and Motion Control Conference, 2008. EPE-PEMC 2008. 13th*, 2008, pp. 108-113.
- [2] B. Ju-Won, R. Myung-Hyo, K. Tae-Jin, Y. Dong-Wook, and K. Jong-Soo, "High boost converter using voltage multiplier," in *Industrial Electronics Society, 2005. IECON 2005. 31st Annual Conference of IEEE*, 2005, p. 6 pp.
- [3] Z. Qun and F. C. Lee, "High-efficiency, high step-up DC-DC converters," *Power Electronics, IEEE Transactions on*, vol. 18, pp. 65-73, 2003.
- [4] W. Rong-Jong and D. Rou-Yong, "High step-up converter with coupled-inductor," *Power Electronics, IEEE Transactions on*, vol. 20, pp. 1025-1035, 2005.
- [5] K. C. Tseng and T. J. Liang, "Novel high-efficiency step-up converter," *Electric Power Applications, IEE Proceedings* -, vol. 151, pp. 182-190, 2004.
- [6] R. J. Wai and R. Y. Duan, "High-efficiency DC/DC converter with high voltage gain," *Electric Power Applications, IEE Proceedings* -, vol. 152, pp. 793-802, 2005.
- [7] G. V. Torrico-Bascope, R. P. Torrico-Bascope, D. S. Oliveira, F. L. M. Antunes, S. V. Araujo, and C. G. C. Branco, "A Generalized High Voltage Gain Boost Converter Based on Three-State Switching Cell," in *The 32nd Annual Conference of the IEEE Industrial Electronics Society IECON'06*, Paris, France, 2006, pp. 1927-1932.
- [8] P. Zacharias, B. Sahan, S. V. Araújo, F. L. M. Antunes, and R. T. Bascope, "Analysis and Proposition of a PV Module Integrated Converter with High Voltage Gain Capability in a non-isolated Topology," in *The 7th International Conference on Power Electronics* Daegu, Korea: IEEE, 2007.
- [9] G. V. T. Bascope and I. Barbi, "Generation of a family of non-isolated DC-DC PWM converters using new three-state switching cells," in *Power Electronics Specialists Conference, 2000. PESC 00. 2000 IEEE 31st Annual*, 2000, pp. 858-863 vol.2.
- [10] E. H. Kim and B. H. Kwon, "High step-up resonant push-pull converter with high efficiency," *Power Electronics, IET*, vol. 2, pp. 79-89, 2009.
- [11] L. Po-Wa, L. Yim-Shu, D. K. W. Cheng, and L. Xiu-Cheng, "Steady-state analysis of an interleaved boost converter with coupled inductors," *Industrial Electronics, IEEE Transactions on*, vol. 47, pp. 787-795, 2000.
- [12] C. W. T. McLyman, *Transformer and inductor design handbook*: Marcel Dekker, 2004.
- [13] J. D. Pollock and C. R. Sullivan, "Gapped-inductor foil windings with low AC and DC resistance," in *Industry Applications Conference, 2004. 39th IAS Annual Meeting. Conference Record of the 2004 IEEE*, 2004, p. 557.
- [14] J. D. Pollock and C. R. Sullivan, "Modelling Foil Winding Configurations with Low AC and DC Resistance," in *Power Electronics Specialists Conference, 2005. PESC '05. IEEE 36th*, 2005, pp. 1507-1512.
- [15] M. Nymand and M. A. E. Andersen, "A new approach to high efficiency in isolated boost converters for high-power low-voltage fuel cell applications," in *Power Electronics and Motion Control Conference, 2008. EPE-PEMC 2008. 13th*, 2008, pp. 127-131.

A.5 Integration of Magnetic Components in a Step-Up Converter for Fuel Cell (EPE 2009)

Integration of Magnetic Components in a Step-Up Converter for Fuel Cell

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Keywords

«DC power supply», «photovoltaic», «renewable energy systems», «switched-mode power supply», «uninterruptible power supply (UPS)»

Abstract

Fuel cell generator is a good example of a high voltage gain application in which dc-dc step-up converter is a critical part. The input voltage of the converter decreases while the output power increases. It creates challenges in design of the converter's magnetic components. Scope of this paper is integration of the dc inductor and the transformer on a single core. Such integration improves utilization of the core and windings. It leads to size reduction of the converter.

Introduction

An increasing interest in alternative and renewable energy creates a demand for novel power conversion systems, which interfaces different energy source to a load or to a utility grid. Very often it's necessary to boost a low voltage from a source (small fuel cells, most of photovoltaic panels) to a high voltage suitable for an inverter. The required voltage gain may exceed value of 20 in many cases. Such gain is attainable for boost converter with SiC diodes and CoolMOS transistors, but by a cost of poor semiconductors utilization and limited efficiency [1]. In the literature [2-6] one may find several topologies with a coupled inductor, which offer a high voltage gain. The main drawback among these topologies is large input current ripple and such ripples may lead to PV maximum power point tracking mismatch or to quick degradation of a fuel cell. For these reasons an additional input filter is required, but it increases size, cost and complexity of the converter. The topology introduced in [7] and presented on Fig. 1 offers a high voltage gain, reduced voltage rating of MOSFETs and input current ripple is limited by inductor L_M . Reference [8, 9] reports a very good performance of this topology in a high voltage gain application, like a fuel cell. However in such application the converter has to operate under variable, load dependent input voltage. Typically for fuel cell minimum to maximum input voltage ratio is about 1:2 [10]. While the converter operates under different conditions it might be difficult to optimize magnetic components. On one hand they are sized for high input current. On the other hand they are designed for the highest input voltage too. But in fuel cell application high voltage and high current doesn't occur at the same time. It may result in poor utilization of magnetic cores of the inductor and the transformer.

The main focus in this paper is to design and implement of an integrated magnetic, which should reduce size and weight of the converter.

Description of the converter

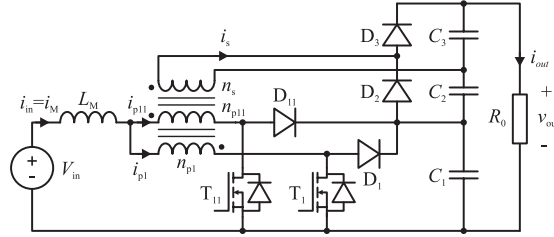


Fig. 1 Diagram of the converter

The selected topology is presented on Fig. 1. It incorporates so called 3-state switching cell (T_1 , T_{11} , D_1 , D_{11} and the transformer) [7, 11]. Explanation of the converter's operation become more intuitive if one considers this topology as a modified current fed push-pull converter – with diodes D_1 , D_{11} and capacitor C_1 as a lossless clamp for transistors. Key waveforms are presented on Fig. 2. Basically the converter operates with transistor duty cycle larger than 50 %, i.e. overlapping mode. Assuming continuous conduction mode (CCM) there are four operating modes. Mode 1 and 3 are identical, while both transistors are turned-on and share the input current equally ($n_{p1}=n_{p11}$). During this period the input inductor L_M is being charged and the input current i_{in} rises. Because both primary windings are shorted there is no voltage across the secondary winding, so there is no current flow in the secondary winding too. Next, in mode 2 the transistor T_1 is being turned-off and energy stored in L_M is being released thru the primary winding (n_{p1}) and the diode D_1 to the capacitor C_1 , and thru the secondary winding n_s and the diode D_3 to the capacitor C_3 . The last mode 4 is symmetrical to mode 2 – while the transistor T_1 remains turned-on and T_{11} is turned-off. During this period the diode D_{11} and the diode D_2 conduct. Capacitors C_1 and C_2 are recharged. Static voltage gain of the converter is given by (1), where n is primary to secondary turns ratio. Voltage stress is given by (2) for the primary side semiconductors and by (3) for the secondary side diodes D_2 and D_3 .

$$V_{out} = \frac{1+n}{1-D} \cdot V_{in} \quad (1)$$

$$V_{T1} = V_{T11} = V_{D1} = V_{D11} = \frac{1}{n+1} \cdot V_{out} \quad (2)$$

$$V_{D2} = V_{D3} = \frac{n}{n+1} \cdot V_{out} \quad (3)$$

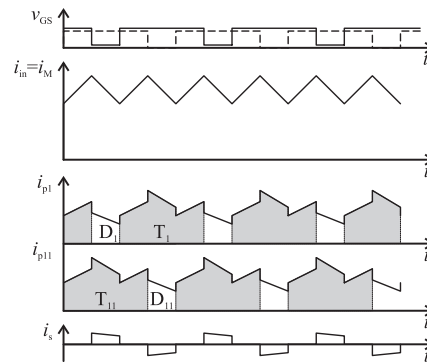


Fig. 2 Main waveforms of the converter

Magnetic components

Magnetic components are essential for any dc-dc converter design. Their performance reflects directly on converter's performance. On the one hand a design of magnetic components focuses on reduction of losses inside them and on reduction of parasitics, so external circuit is not affected. On the other hand magnetic components are significant part of the converter size and weight, so size reduction should be taken into consideration too. In many cases integration of magnetics may improve utilization of a core or windings and thus size may be reduced.

The dc inductor

In the considered topology the dc inductor L_M conducts essentially the dc current with relatively small ac component (ripples). Majority of dc current content allows using of a round wire for the inductor winding. It characterizes relatively low cost and good copper fill factor K_u . Since the dc current is dominant a low dc resistance is a key. In order to improve copper fill factor one may use two or three thinner wires in parallel or a rectangular wire instead of a single thick round wire. If required number of turns is low one may use a foil winding, which may provide a very good copper fill factor and thus a very low dc resistance [9].

A design procedure based on area-product approach is well described in [12], so here only major steps are presented. First, the required inductance L_M is to be determined. For the considered converter it's given by (4), where ΔI_M is the amplitude of current ripples. By rearranging (4) it's found that the largest current ripples occur at the duty cycle $D=0.75$.

$$L_M = \frac{V_{out} \cdot (D - 0.5) \cdot (1 - D)}{f_s \cdot 2 \cdot \Delta I_M \cdot (1 + n)} \quad (4)$$

Assuming that the inductor operates in its linear region, below saturation it's easy to find dc and ac induction components (B_{ind} and ΔB_{ind}) since they are directly proportional to the inductor dc and ac current components ($I_{M(dc)}$ and ΔI_M).

The core size is characterized by the area product A_p , which is the product of the core cross section area A_c and the window area W_a [13]. Required area product A_p value is given by (5). The current $I_{M(dc)}$ is the inductor maximum dc current, i.e. at the minimum input voltage V_{in} and rated power. When the dimensions of the core are known one may find required number of turns (6) and length of the air gap (7).

$$A_p = \frac{L_M \cdot I_{M(dc)} \cdot (I_{M(dc)} + \Delta I_M)}{(B_{ind} + \Delta B_{ind}) \cdot J \cdot K_u} \quad (5)$$

$$n_M = \frac{L_M \cdot \Delta I_M}{\Delta B_{ind} \cdot A_c} \quad (6)$$

$$l_g = \frac{\mu_0 \cdot n_M^2 \cdot A_c}{L_M} \quad (7)$$

For small air gaps effective area of the gap A_g is close to core cross section area A_c (8). For larger gaps the effective area of the gap increases and have to be corrected according to (9) [12].

$$A_g \simeq A_c = a \cdot b \quad (8)$$

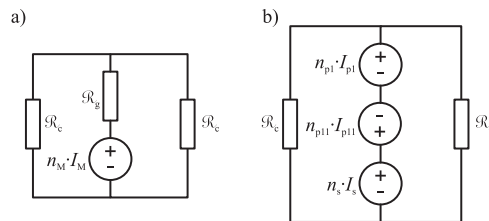


Fig. 3 Magnetic circuits of an inductor (a) and a push-pull transformer (b)

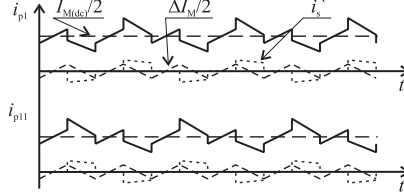


Fig. 4 The transformer primary currents and its components

$$A_g \approx (a + l_g) \cdot (b + l_g) \quad (9)$$

Equivalent magnetic circuit of the inductor is presented on Fig. 3a. Magneto-motive force (MMF) is represented as voltage source $n_M \cdot I_M$, while the air gap reluctance is represented by linear resistor \mathcal{R}_g . Resistor \mathcal{R}_c represents reluctance of the ferrite core and it's very small in compare to reluctance of the air gap ($\mathcal{R}_c \ll \mathcal{R}_g$).

The push-pull transformer

Fig. 4 presents the transformer primary currents and its components: input dc current $I_{M(dc)}$, input current ripples ΔI_M and reflected secondary current i_s' . This combination of ac and dc components creates challenge for design of the transformer windings. Reduction of both, dc and ac resistances of primary windings is crucial. Use of a Litz wire helps to reduce skin and proximity effects. Unfortunately in the same time the Litz wire has poor copper fill factor K_u , so one end up with a bulky transformer or a large dc resistance. Also the leakage inductance of such a winding is relatively high affecting the external circuit. Round wire has a better copper fill factor and dc resistance is reduced in compare to Litz wire. However inappropriate design of such windings may result in significant ac losses due to the skin and proximity effects. Interleaving of the primary and the secondary windings helps to reduce ac losses. A foil winding may provide a very good copper fill factor and a low dc resistance. Interleaved winding arrangement a large area of the primary and the secondary winding facing each other, thus the ac resistance is reduced. Unfortunately, in the same time interwinding capacitance increases. For a few turns and thick isolation between primary and the secondary it may not be a severe problem and such design will have a very good performance [9]. But reduction of the isolation thickness and thus the distance between the primary and the secondary winding may result in significant increases of the interwinding. A large interwinding capacitance results in a significant degradation of the converter's performance.

Design procedure based on area product A_p is described in details in [12]. First, size of the core is calculated from (10). Variable P_t is transformer apparent power, i.e. sum of input and output power of the transformer.

$$A_p = \frac{P_t}{2 \cdot K_u \cdot K_f \cdot \Delta B_{tr} \cdot J \cdot f_s} \quad (10)$$

Induction amplitude ΔB_{tr} may not exceed saturation level of the core. However in many cases the peak induction is well below the saturation level because of the maximum allowed core loss. Specific core loss P_{fe} as a function of induction amplitude and switching frequency is given by well known Steinmetz equation [13]. Once the induction amplitude ΔB_{tr} and the core size are known the number of primary turns can be found with (11). It's found that the largest induction amplitude occurs at duty cycle $D=0.5$, i.e. for the highest input voltage.

$$n_{p1} = n_{p11} = \frac{1}{2 \cdot \Delta B_{tr} \cdot A_c} \cdot \frac{V_{out}}{2 \cdot (1+n)} \cdot \frac{1-D}{f_s} \quad (11)$$

Fig. 3b shows the magnetic circuit of a push-pull transformer. There are three voltage sources representing MMFs of windings. MMFs directions refer to the converter diagram on Fig. 1. Reluctance of the core is represented by the resistor \mathcal{R}_c . By analyzing primary current's (Fig. 4) one can find that MMFs caused by the input current (dc and ac components) cancel each other. There is

no effect in the secondary winding due to the input current components flowing in the primary windings.

The integrated magnetic

There are two major reasons for integration of the inductor and the transformer into a single device. First, the high frequency transformer is a thermal limited design, so the induction amplitude ΔB_{tr} might be well below the core saturation level. It leaves some room for dc flux which may come from the inductor winding n_M . Second, the input current flows thru the primary windings of the push-pull transformer but creates no flux since MMFs related to the primary windings are opposite. The only result of the input current flow in the primary windings is a copper loss. However with a proper winding arrangement it's possible to use primary windings as a part of the inductor windings.

Fig. 3 presents magnetic circuits of the inductor and the push-pull transformer. These two circuits can be combined together on a single EE core. The simplest way is to place the inductor winding n_M on the center gapped leg. Transformer windings are split into two identical halves and placed on outer legs. Resulting magnetic circuit is shown on Fig. 5. In this way the inductor and the transformer fluxes are present in the outer legs of the core, which improves its utilization. However the flux generated by inductor winding does not affect transformer windings. Also flux generated by the transformer has no influence on the inductor. This solution results in complex winding arrangement, large overall number of turns and possible large winding resistances.

The inductor current splits into two halves in the transformer primary windings. The flux related to the inductor winding also splits into two halves once it goes into the core outer legs. So, there is a great agreement between inductor current, the transformer primary current components ($I_{M(dc)}$ and ΔI_M) and related fluxes. It's possible to use the transformer primary windings as a part of the inductor winding. For proper operation of the transformer the secondary winding is split and arranged on both outer legs, so it's not affected by inductor flux. Proposed magnetic circuit is presented on Fig. 6 where currents directions refer to Fig. 1. The magnetic circuit from Fig. 6 is described by (12), where L_M is self inductance of n_M winding, M_{Mp1} is mutual inductance between n_M and n_{p1} windings and so on.

Design of the integrated magnetic is an iterative process. When both transistors are turned-on the input voltage is applied to inductor and transformer's primary windings, so (13) is truth. Assuming that secondary current is zero and both primary currents are equal $i_{p1}=i_{p11}$ one can write (14) and (15). Combining these equations with (13) gives the equivalent inductance L_{Meq} (16). With a good

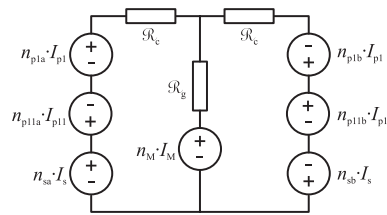


Fig. 5 Magnetic circuit of the integrated inductor-transformer

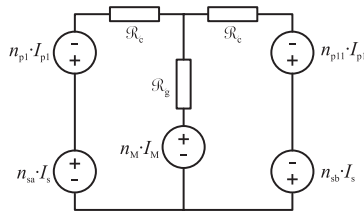


Fig. 6 Reduced magnetic circuit of the integrated inductor-transformer

coupling between both primary windings the mutual inductance M_{p1p11} value is close to the self inductance L_{p1} value, so they will cancel each other. It's important to note that the equivalent inductance L_{Meq} is larger than the physical inductance L_M , so in this way the inductance L_M may be reduced. It turns into fewer inductor turns n_M and possibly lower conduction losses.

Approximated core size is found using area product approach simply by summarizing area products required by the transformer and by the inductor (17). One can change ratio between the inductor induction B_{ind} and the transformer induction ΔB_{tr} and find the minimum required core size. This method gives only an approximated core size, but it's a good starting point for further optimization and the size reduction.

Once the core size is determined the inductor and the transformer windings are designed according to guidelines presented in previous sections. First, number of turns in the transformer primary winding is found with (11). Next, in an iterative process one can calculate self inductances and mutual inductances (12), find required number of turns n_M (6) and size of the air gap l_g (7).

Contrary to a typical transformer, the integrated magnetic usually operates under significant dc flux conditions. It has two major effects. First, because of dc flux in the core increased core losses may occur. Unfortunately core datasheets contain power loss data only for pure sinusoidal excitation, so it's difficult to calculate core losses in advance. Second, the peak induction is higher in compare to a traditional transformer. Thus there is a very little space for any undesired dc flux. It requires careful control of dc currents flowing thru primary windings n_{p1} and n_{p11} .

$$\begin{bmatrix} v_M \\ v_{p1} \\ v_{p11} \\ v_{sa} \\ v_{sb} \end{bmatrix} = \begin{bmatrix} L_M & M_{Mp1} & M_{Mp11} & -M_{Msa} & M_{Msb} \\ M_{p1M} & L_{p1} & -M_{p1p11} & -M_{p1sa} & -M_{p1sb} \\ M_{p11M} & -M_{p11p1} & L_{p11} & M_{p11sa} & M_{p11sb} \\ -M_{saM} & -M_{sap1} & M_{sap11} & L_{sa} & M_{sasb} \\ M_{sbM} & -M_{sbp1} & M_{sbp11} & M_{sbsa} & L_{sb} \end{bmatrix} \cdot \begin{bmatrix} \frac{di_M}{dt} \\ \frac{di_{p1}}{dt} \\ \frac{di_{p11}}{dt} \\ \frac{di_{sa}}{dt} \\ \frac{di_{sb}}{dt} \end{bmatrix} \quad (12)$$

$$v_{in} = v_M + v_{p1} = L_{Meq} \cdot \frac{di_M}{dt} \quad (13)$$

$$v_M = L_M \cdot \frac{di_M}{dt} + M_{Mp1} \cdot \frac{di_{p1}}{dt} + M_{Mp11} \cdot \frac{di_{p11}}{dt} \quad (14)$$

$$v_{p1} = M_{p1M} \cdot \frac{di_M}{dt} + L_{p1} \cdot \frac{di_{p1}}{dt} - M_{p1p11} \cdot \frac{di_{p11}}{dt} \quad (15)$$

$$L_{Meq} = L_M + M_{Mp1} + M_{p1M} + \frac{1}{2} \cdot L_{p1} - \frac{1}{2} \cdot M_{p1p11} \quad (16)$$

$$A_p = \frac{P_t}{2 \cdot K_u \cdot K_f \cdot \Delta B_{tr} \cdot J \cdot f_s} + \frac{L_{Meq} \cdot I_{M(dc)} \cdot (I_{M(dc)} + \Delta I_M)}{(B_{ind} + \Delta B_{ind}) \cdot J \cdot K_u} \quad (17)$$

Experimental setup and results

In order to verify theoretical analysis and calculations the 500 W breadboard is built and tested. The input voltage varies from 30 to 50 Vdc and the output voltage is regulated at 400 Vdc. The switching frequency is $f_s=50$ kHz and the transformer turns ratio is $n=2$. According to (2) it allows using 150 V MOSFETs (IRFP4321PbF) and 150 V Schottky diodes (30CPQ150PbF) on primary side. On the secondary side of the transformer there are 600 V SiC diodes (IDT10S60C).

It's found that the E42/21 core (0P44022EC) is sufficiently large. With $n_M=10$ turns and 1.8 mm air gap in the center leg it gives the inductance $L_M=18$ μ H. The transformer induction amplitude is limited to $\Delta B_{tr}=0.15$ T at the highest input voltage and it's limited by core losses. The transformer primary winding has $n_{p1}=n_{p11}=13$ turns, which results in the equivalent inductance $L_{Meq}=48$ μ H. The secondary winding has $n_s=26$ turns and it's divided into halves, $n_{sa}=n_{sb}=13$ turns on each of outer legs. The primary and the secondary windings are interleaved to reduce proximity effect and ac losses. The assembled integrated inductor transformer is presented on Fig. 7. Fig. 8 presents the



Fig. 7 The integrated inductor-transformer (core type EE42/21)

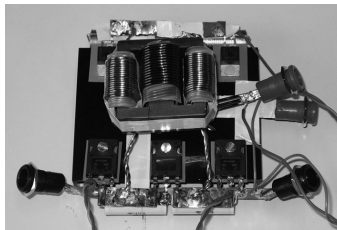


Fig. 8 The assembled 500 W step-up converter

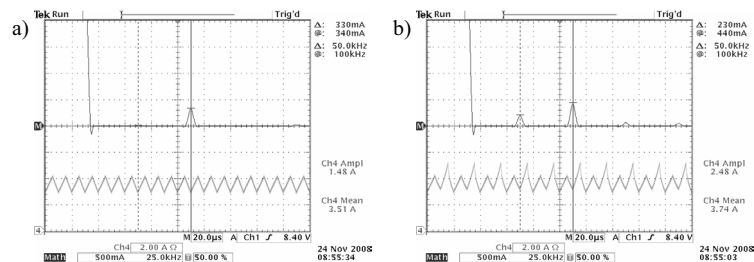


Fig. 9 The observed input current and its spectrum in balances case (left) and in case of saturation of the other leg (right)

assembled 500 W converter. Below the integrated transformer-inductor two MOSFETs (T_1 , T_{11}) and diodes (D_1 , D_{11} in a single pack) are visible. Control of dc currents in primary windings is critical to avoid outer legs saturation. In case of integrated inductor-transformer it's possible to detect such saturation by observation of the input current only. Fig. 9a shows the input current and its spectrum in an unsaturated and balanced case. The input current has only a large dc component and 100 kHz component, which refers to input current ripples at double switching frequency. In case of small unbalance of the transformer primary currents one of outer legs become saturated and shape of the input current changes. Now, 50 kHz component appears in the current spectrum, like presented on Fig. 9b.

Fig. 10 presents measured efficiency of the converter at 30 V and 45 V input voltage. For the lower input voltage the efficiency peaks at 97.4% at 250 W and remains above 97% up to 450 W. For the higher input voltage the efficiency exceeds 97.5%.

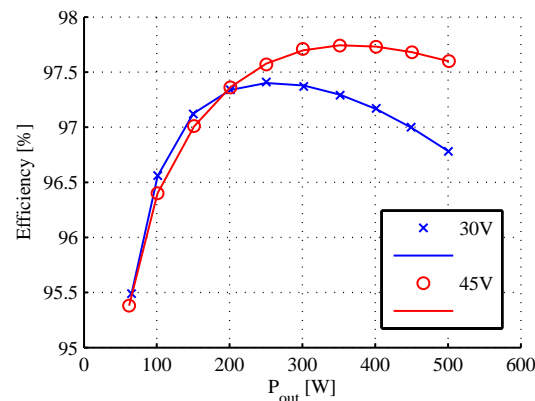


Fig. 10 Measured efficiency of the converter

Conclusion

A boost converter with a three state switching cell and integrated magnetic has been presented in this paper. The converter has the inductor and the push-pull transformer arranged on a standard gapped EE core. Such integration allows using of transformer primary windings as a part of the inductor winding, thus smaller physical inductance is required. It results in smaller and lighter core. To verify the idea the 500 W breadboard is built and tested. The breadboard exhibits a good performance and a compact assembly.

References

- [1] P. Klimczak and S. Munk-Nielsen, "Comparative study on paralleled vs. scaled dc-dc converters in high voltage gain applications," in *Power Electronics and Motion Control Conference, 2008. EPE-PEMC 2008. 13th*, 2008, pp. 108-113.
- [2] B. Ju-Won, R. Myung-Hyo, K. Tae-Jin, Y. Dong-Wook, and K. Jong-Soo, "High boost converter using voltage multiplier," in *Industrial Electronics Society, 2005. IECON 2005. 31st Annual Conference of IEEE*, 2005, p. 6 pp.
- [3] Z. Qun and F. C. Lee, "High-efficiency, high step-up DC-DC converters," *Power Electronics, IEEE Transactions on*, vol. 18, pp. 65-73, 2003.
- [4] W. Rong-Jong and D. Rou-Yong, "High step-up converter with coupled-inductor," *Power Electronics, IEEE Transactions on*, vol. 20, pp. 1025-1035, 2005.
- [5] K. C. Tseng and T. J. Liang, "Novel high-efficiency step-up converter," *Electric Power Applications, IEE Proceedings* -, vol. 151, pp. 182-190, 2004.
- [6] R. J. Wai and R. Y. Duan, "High-efficiency DC/DC converter with high voltage gain," *Electric Power Applications, IEE Proceedings* -, vol. 152, pp. 793-802, 2005.
- [7] G. V. Torrico-Bascope, R. P. Torrico-Bascope, D. S. Oliveira, F. L. M. Antunes, S. V. Araujo, and C. G. C. Branco, "A Generalized High Voltage Gain Boost Converter Based on Three-State Switching Cell," in *The 32nd Annual Conference of the IEEE Industrial Electronics Society IECON'06*, Paris, France, 2006, pp. 1927-1932.
- [8] P. Zacharias, B. Sahan, S. V. Araújo, F. L. M. Antunes, and R. T. Bascopé, "Analysis and Proposition of a PV Module Integrated Converter with High Voltage Gain Capability in a non-isolated Topology," in *The 7th International Conference on Power Electronics Daegu, Korea: IEEE*, 2007.
- [9] P. Klimczak and S. Munk-Nielsen, "High Efficiency Boost Converter with Three State Switching Cell," in *International Exhibition & Conference for Power Electronics, Intelligent Motion, Power Quality PCIM Europe 2009 Nuremberg, Germany*, 2009.
- [10] W. Vielstich, *Handbook of fuel cells fundamentals, technology, and applications* editors, Wolf Vielstich, Arnold Lamm, Hubert A. Gasteiger: Wiley, 2003.

- [11] G. V. T. Bascope and I. Barbi, "Generation of a family of non-isolated DC-DC PWM converters using new three-state switching cells," in *Power Electronics Specialists Conference, 2000. PESC 00. 2000 IEEE 31st Annual*, 2000, pp. 858-863 vol.2.
- [12] C. W. T. McLyman, *Transformer and inductor design handbook*: Marcel Dekker, 2004.
- [13] J. Reinert, A. Brockmeyer, and R. W. A. A. De Doncker, "Calculation of losses in ferro- and ferrimagnetic materials based on the modified Steinmetz equation," *Industry Applications, IEEE Transactions on*, vol. 37, pp. 1055-1061, 2001.

Appendix B

Models

B.1 Transistor loss model (lib_trans.m)

```

1  %Calculation of transistor conduction, switching and gate losses
2  %INPUT DATA FROM CONVERTER FILE
3  trans_model;
4  trans_Tj;
5  trans_fs;
6  trans_Von;
7  trans_Voff;
8  trans_Ion;
9  trans_Ioff;
10 trans_VGS;
11 trans_Rgon;
12 trans_Rgoff;
13 trans_Irms;
14
15 %INPUT DATA FROM DATA FILE
16 trans_RDson=trans.RDson(trans_model)+(trans_Tj-
17 25)*trans.Rtemp(trans_model);
18 trans_Cgs=trans.Cgs(trans_model);
19 trans_Cosse=trans.Cosse(trans_model);
20 trans_Coss=[trans.Coss0(trans_model), trans.Coss1(trans_model),
21 trans.Coss2(trans_model) trans.Coss3(trans_model)];
22 trans_Crss=[trans.Crss0(trans_model), trans.Crss1(trans_model),
23 trans.Crss2(trans_model) trans.Crss3(trans_model)];
24 trans_VDS=[trans.VDS0(trans_model), trans.VDS1(trans_model),
25 trans.VDS2(trans_model) trans.VDS3(trans_model)];
26 trans_Rgontot=trans.Rgint(trans_model)+trans_Rgon;
27 trans_Rgofftot=trans.Rgint(trans_model)+trans_Rgoff;
28 trans_Qg=trans.Qg(trans_model);
29 trans_Qmill=trans.Qmill(trans_model);
30 trans_VGSth=trans.VGSth(trans_model);
31 trans_gfs=trans.gfs(trans_model);
32
33 %Switching times calculation
34 trans_Ciss=trans_Cgs+interp1(trans_VDS,trans_Crss,trans_Von,'pchip
35 ');
36
37 %Turn-on delay time
38 trans_tdon=trans_Rgontot*trans_Ciss*log((trans_VGS)/(trans_VGS-
39 trans_VGSth));
40
41 %Current rise time
42 trans_tir=trans_Rgontot*trans_Ciss*log((trans_VGS-
43 trans_VGSth)/(trans_VGS-trans_VGSth-trans_Ion/trans_gfs));
44

```

```

36 %Energy dissipated during voltage fall time
37 trans_Vvf_mx=linspace(trans_Von,trans_Ion*trans_RDson,100);
38 trans_tvf_mx=0;
39 trans_Evf=0;
40 for trans_i=2:size(trans_Vvf_mx,2)
41 %Volt fall time estimation due to Cgd (gate side) behavior
42 trans_Cgd=interp1(trans_VDS,trans_Crss,trans_Vvf_mx(trans_i),'pchip');
43 trans_tvf_mx(trans_i)=trans_tvf_mx(trans_i-1)+(trans_Vvf_mx(trans_i)-trans_Vvf_mx(trans_i-1))*trans_Rgontot*trans_Cgd/(trans_VGS-trans_VGsth-trans_Ion/trans_gfs);
44 trans_Evf=trans_Evf+(trans_tvf_mx(trans_i)-trans_tvf_mx(trans_i-1))*trans_Ion*trans_Vvf_mx(trans_i);
45 end
46 trans_PTon=trans_fs*trans_Ion*trans_Von*trans_tir/2+trans_Evf*trans_fs;
47
48 %turn-off transient
49 trans_Ciss=trans_Cgs+interp1(trans_VDS,trans_Crss,trans_Voff,'pchip');
50 %Turn-off delay time
51 trans_tdoff=trans_Rgofftot*trans_Ciss*log((trans_VGS)/(trans_VGsth+trans_Ioff/trans_gfs));
52 %Current fall time
53 trans_tif=trans_Rgofftot*trans_Ciss*log((trans_VGsth+trans_Ioff/trans_gfs)/(trans_VGsth));
54
55 %Energy dissipated during voltage rise time
56 trans_Vvr_mx=linspace(trans_Ioff*trans_RDson,trans_Voff,100);
57 trans_tvr_mx=0;
58 trans_Evr=0;
59 for trans_i=2:size(trans_Vvr_mx,2)
60 %Volt rise time estimation due to the Cgd (gate side) behavior
61 trans_Cgd=interp1(trans_VDS,trans_Crss,trans_Vvr_mx(trans_i),'pchip');
62 trans_tvr_mx(trans_i)=trans_tvr_mx(trans_i-1)+(trans_Vvr_mx(trans_i)-trans_Vvr_mx(trans_i-1))*trans_Rgofftot*trans_Cgd/(trans_VGsth+trans_Ion/trans_gfs);
63 trans_Evr=trans_Evr+(trans_tvr_mx(trans_i)-trans_tvr_mx(trans_i-1))*trans_Ioff*trans_Vvr_mx(trans_i);
64 end
65 trans_PToff=trans_fs*trans_Ioff*trans_Voff*trans_tif/2+trans_Evr*trans_fs;
66
67 %on-state losses
68 trans_PTcond=trans_Irms^2*trans_RDson;
69
70 %gate drive losses
71 trans_PTgate=trans_VGS*trans_Qg*trans_fs;

```

B.2 Transistor data library (data_trans.m)

```

1 %MOSFET database
2 trans_i=1;

```

```

3   trans.type(trans_i)=[ '01.ideal MOSFET' ];
4   trans.Vbrr(trans_i)=inf; %V
5   trans.Id(trans_i)=inf; %A
6   trans.RDSon(trans_i)=0; %ohm
7   trans.Rtemp(trans_i)=0; %ohm/K
8   trans.VDS0(trans_i)=1; %V
9   trans.VDS1(trans_i)=10; %V
10  trans.VDS2(trans_i)=1e3; %V
11  trans.VDS3(trans_i)=1e6; %V
12  trans.Coss0(trans_i)=0; %F
13  trans.Coss1(trans_i)=0; %F
14  trans.Coss2(trans_i)=0; %F
15  trans.Coss3(trans_i)=0; %F
16  trans.Crss0(trans_i)=0; %F
17  trans.Crss1(trans_i)=0; %F
18  trans.Crss2(trans_i)=0; %F
19  trans.Crss3(trans_i)=0; %F
20  trans.Cosse(trans_i)=0; %F
21  trans.Cgs(trans_i)=0; %F
22  trans.Rgint(trans_i)=0; %ohm
23  trans.Qg(trans_i)=0e-9; %C
24  trans.Qmill(trans_i)=0e-9; %C
25  trans.VGSth(trans_i)=0; %V
26  trans.gfs(trans_i)=1e3; %S
27
28  trans_i=trans_i+1;
29  trans.type(trans_i)=[ '02.ipw60r045cp' ];
30  trans.Vbrr(trans_i)=650;
31  trans.Id(trans_i)=60;
32  trans.RDSon(trans_i)=40e-3;
33  trans.Rtemp(trans_i)=.56e-3;
34  trans.VDS0(trans_i)=5;
35  trans.VDS1(trans_i)=50;
36  trans.VDS2(trans_i)=150;
37  trans.VDS3(trans_i)=450;
38  trans.Coss0(trans_i)=17000e-12;
39  trans.Coss1(trans_i)=800e-12;
40  trans.Coss2(trans_i)=250e-12;
41  trans.Coss3(trans_i)=210e-12;
42  trans.Crss0(trans_i)=1000e-12;
43  trans.Crss1(trans_i)=90e-12;
44  trans.Crss2(trans_i)=5e-12;
45  trans.Crss3(trans_i)=5e-12;
46  trans.Cosse(trans_i)=320e-12;
47  trans.Cgs(trans_i)=6800e-12;
48  trans.Rgint(trans_i)=1;
49  trans.Qg(trans_i)=150e-9;
50  trans.Qmill(trans_i)=50e-9;
51  trans.VGSth(trans_i)=3;
52  trans.gfs(trans_i)=60;
53
54  trans_i=trans_i+1;
55  trans.type(trans_i)=[ '03.irfb4228pbf' ];
56  trans.Vbrr(trans_i)=150;
57  trans.Id(trans_i)=180;
58  trans.RDSon(trans_i)=12e-3;
59  trans.Rtemp(trans_i)=.15e-3;
60  trans.VDS0(trans_i)=2;

```

```
61  trans.VDS1(trans_i)=10;
62  trans.VDS2(trans_i)=50;
63  trans.VDS3(trans_i)=150;
64  trans.Coss0(trans_i)=3000e-12;
65  trans.Coss1(trans_i)=900e-12;
66  trans.Coss2(trans_i)=400e-12;
67  trans.Coss3(trans_i)=250e-12;
68  trans.Crss0(trans_i)=600e-12;
69  trans.Crss1(trans_i)=170e-12;
70  trans.Crss2(trans_i)=90e-12;
71  trans.Crss3(trans_i)=67e-12;
72  trans.Cosse(trans_i)=480e-12;
73  trans.Cgs(trans_i)=4530e-12;
74  trans.Rgint(trans_i)=1;
75  trans.Qg(trans_i)=72e-9;
76  trans.Qmill(trans_i)=30e-9;
77  trans.VGSth(trans_i)=5;
78  trans.gfs(trans_i)=170;
79
80  trans_i=trans_i+1;
81  trans.type(trans_i)=[ '04.fch47n60' ];
82  trans.Vbrr(trans_i)=600;
83  trans.Id(trans_i)=47;
84  trans.RDSon(trans_i)=58e-3;
85  trans.Rtemp(trans_i)=.17e-3;
86  trans.VDS0(trans_i)=1;
87  trans.VDS1(trans_i)=25;
88  trans.VDS2(trans_i)=50;
89  trans.VDS3(trans_i)=480;
90  trans.Coss0(trans_i)=15000e-12;
91  trans.Coss1(trans_i)=3200e-12;
92  trans.Coss2(trans_i)=1150e-12;
93  trans.Coss3(trans_i)=160e-12;
94  trans.Crss0(trans_i)=3000e-12;
95  trans.Crss1(trans_i)=300e-12;
96  trans.Crss2(trans_i)=10e-12;
97  trans.Crss3(trans_i)=10e-12;
98  trans.Cosse(trans_i)=420e-12;
99  trans.Cgs(trans_i)=8000e-12;
100 trans.Rgint(trans_i)=1;
101 trans.Qg(trans_i)=210e-9;
102 trans.Qmill(trans_i)=120e-9;
103 trans.VGSth(trans_i)=3;
104 trans.gfs(trans_i)=40;
105 trans_i=trans_i+1;
106
107 trans.type(trans_i)=[ '05.fdb2532' ];
108 trans.Vbrr(trans_i)=150;
109 trans.Id(trans_i)=79;
110 trans.RDSon(trans_i)=14e-3;
111 trans.Rtemp(trans_i)=.17e-3;
112 trans.VDS0(trans_i)=1;
113 trans.VDS1(trans_i)=10;
114 trans.VDS2(trans_i)=50;
115 trans.VDS3(trans_i)=150;
116 trans.Coss0(trans_i)=3300e-12;
117 trans.Coss1(trans_i)=1050e-12;
118 trans.Coss2(trans_i)=380e-12;
```

```
119 trans.Coss3(trans_i)=290e-12;
120 trans.Crss0(trans_i)=660e-12;
121 trans.Crss1(trans_i)=220e-12;
122 trans.Crss2(trans_i)=95e-12;
123 trans.Crss3(trans_i)=50e-12;
124 trans.Cosse(trans_i)=615e-12;
125 trans.Cgs(trans_i)=6000e-12;
126 trans.Rgint(trans_i)=1;
127 trans.Qg(trans_i)=82e-9;
128 trans.Qmill(trans_i)=19e-9;
129 trans.VGsth(trans_i)=3;
130 trans.gfs(trans_i)=105;
131
132 trans_i=trans_i+1;
133 trans.type(trans_i)=[ '06.irfp4321pbf' ];
134 trans.Vbrr(trans_i)=150;
135 trans.Id(trans_i)=78;
136 trans.RDSon(trans_i)=12e-3;
137 trans.Rtemp(trans_i)=.19e-3;
138 trans.VDS0(trans_i)=1;
139 trans.VDS1(trans_i)=5;
140 trans.VDS2(trans_i)=10;
141 trans.VDS3(trans_i)=150;
142 trans.Coss0(trans_i)=4000e-12;
143 trans.Coss1(trans_i)=1300e-12;
144 trans.Coss2(trans_i)=900e-12;
145 trans.Coss3(trans_i)=270e-12;
146 trans.Crss0(trans_i)=950e-12;
147 trans.Crss1(trans_i)=200e-12;
148 trans.Crss2(trans_i)=100e-12;
149 trans.Crss3(trans_i)=50e-12;
150 trans.Cosse(trans_i)=390e-12;
151 trans.Cgs(trans_i)=4400e-12;
152 trans.Rgint(trans_i)=1;
153 trans.Qg(trans_i)=71e-9;
154 trans.Qmill(trans_i)=21e-9;
155 trans.VGsth(trans_i)=4.5;
156 trans.gfs(trans_i)=130;
157
158 trans_i=trans_i+1;
159 trans.type(trans_i)=[ '07.irf4568pbf' ];
160 trans.Vbrr(trans_i)=150;
161 trans.Id(trans_i)=171;
162 trans.RDSon(trans_i)=4.8e-3;
163 trans.Rtemp(trans_i)=.06e-3;
164 trans.VDS0(trans_i)=1;
165 trans.VDS1(trans_i)=10;
166 trans.VDS2(trans_i)=50;
167 trans.VDS3(trans_i)=150;
168 trans.Coss0(trans_i)=8000e-12;
169 trans.Coss1(trans_i)=1200e-12;
170 trans.Coss2(trans_i)=1000e-12;
171 trans.Coss3(trans_i)=600e-12;
172 trans.Crss0(trans_i)=11000e-12;
173 trans.Crss1(trans_i)=3500e-12;
174 trans.Crss2(trans_i)=190e-12;
175 trans.Crss3(trans_i)=150e-12;
176 trans.Cosse(trans_i)=977e-12;
```

```
177 trans.Cgs(trans_i)=10470e-12;
178 trans.Rgint(trans_i)=1;
179 trans.Qg(trans_i)=151e-9;
180 trans.Qmill(trans_i)=55e-9;
181 trans.VGsth(trans_i)=3.5;
182 trans.gfs(trans_i)=160;
```

B.3 Diode loss model (lib_diode.m)

```
1 %Calculation of diode losses (conduction, rev.recovery and
  capacitive)
2 %INPUT DATA FROM CONVERTER FILE
3 diode_model;
4 diode_Tj;
5 diode_I;
6 diode_Irms;
7 diode_Ioff;
8 diode_Voff;
9 diode_fs;
10
11 %INPUT DATA FROM DATA FILE
12 diode_Vf=diode.Vf(diode_model)+(diode_Tj-
  25)*diode.Vftemp(diode_model); %for temp<>25C
13 diode_Rf=diode.Rf(diode_model)+(diode_Tj-
  25)*diode.Rftemp(diode_model); %for temp<>25C
14 diode_Qrr=diode.Qrr(diode_model);
15 diode_trr=diode.trr(diode_model);
16 diode_C=[diode.C0(diode_model), diode.C1(diode_model),
  diode.C2(diode_model), diode.C3(diode_model)];
17 diode_VR=[diode.VR0(diode_model), diode.VR1(diode_model),
  diode.VR2(diode_model), diode.VR3(diode_model)];
18
19 %Conduction power losses
20 diode_PDcond=diode_I*diode_Vf+diode_Irms^2*diode_Rf;
21
22 %Reverse recovery losses
23 diode_PDrr=diode_fs*(diode_Voff*diode_Ioff*diode_trr+diode_Voff*di
  ode_Qrr);
24
25 %Diode capacitive loss
26 diode_VR_mx=linspace(0,diode_Voff);
27 diode_QC=0;
28 for diode_i=1:(size(diode_VR_mx,2)-1)
29 diode_QC=diode_QC+interp1(diode_VR, diode_C,
  diode_VR_mx(diode_i), 'pchip')*(diode_VR_mx(diode_i+1)-
  diode_VR_mx(diode_i));
30 end
31 diode_PDC=diode_QC*diode_Voff/2*diode_fs;
```

B.4 Diode data library (data_diode.m)

```
1 %Diode database
2 diode_i=1;
```

```

3   diode.type(diode_i)=(['01.ideal_D']);
4   diode.Vrrm(diode_i)=inf; %V
5   diode.If(diode_i)=inf; %A
6   diode.Vf(diode_i)=0; %V
7   diode.Vftemp(diode_i)=0; %V/K
8   diode.Rf(diode_i)=0; %ohm
9   diode.Rftemp(diode_i)=0; %ohm/K
10  diode.Qrr(diode_i)=0; %C
11  diode.trr(diode_i)=0; %s
12  diode.VR0(diode_i)=0; %V
13  diode.VR1(diode_i)=1; %V
14  diode.VR2(diode_i)=100; %V
15  diode.VR3(diode_i)=1e6; %V
16  diode.C0(diode_i)=0; %F
17  diode.C1(diode_i)=0; %F
18  diode.C2(diode_i)=0; %F
19  diode.C3(diode_i)=0; %F
20
21  diode_i=diode_i+1;
22  diode.type(diode_i)=(['02.sdb06s60']);
23  diode.Vrrm(diode_i)=600;
24  diode.If(diode_i)=6;
25  diode.Vf(diode_i)=.9;
26  diode.Vftemp(diode_i)=-.88e-3;
27  diode.Rf(diode_i)=92e-3;
28  diode.Rftemp(diode_i)=.368e-3;
29  diode.Qrr(diode_i)=21e-9;
30  diode.trr(diode_i)=0;
31  diode.VR0(diode_i)=1;
32  diode.VR1(diode_i)=10;
33  diode.VR2(diode_i)=100;
34  diode.VR3(diode_i)=600;
35  diode.C0(diode_i)=220e-12;
36  diode.C1(diode_i)=90e-12;
37  diode.C2(diode_i)=30e-12;
38  diode.C3(diode_i)=15e-12;
39
40  diode_i=diode_i+1;
41  diode.type(diode_i)=(['03.idt10s60']);
42  diode.Vrrm(diode_i)=600;
43  diode.If(diode_i)=10;
44  diode.Vf(diode_i)=.9;
45  diode.Vftemp(diode_i)=-1e-3;
46  diode.Rf(diode_i)=50e-3;
47  diode.Rftemp(diode_i)=.21e-3;
48  diode.Qrr(diode_i)=0;
49  diode.trr(diode_i)=0;
50  diode.VR0(diode_i)=1;
51  diode.VR1(diode_i)=10;
52  diode.VR2(diode_i)=100;
53  diode.VR3(diode_i)=600;
54  diode.C0(diode_i)=470e-12;
55  diode.C1(diode_i)=245e-12;
56  diode.C2(diode_i)=90e-12;
57  diode.C3(diode_i)=60e-12;
58
59  diode_i=diode_i+1;
60  diode.type(diode_i)=(['04.30cpq150']);

```

```
61 diode.Vrrm(diode_i)=150;
62 diode.If(diode_i)=30;
63 diode.Vf(diode_i)=.5;
64 diode.Vftemp(diode_i)=-1.5e-3;
65 diode.Rf(diode_i)=29e-3;
66 diode.Rftemp(diode_i)=-.08e-3;
67 diode.Qrr(diode_i)=0;
68 diode.trr(diode_i)=0;
69 diode.VR0(diode_i)=5;
70 diode.VR1(diode_i)=15;
71 diode.VR2(diode_i)=45;
72 diode.VR3(diode_i)=150;
73 diode.C0(diode_i)=280e-12;
74 diode.C1(diode_i)=170e-12;
75 diode.C2(diode_i)=95e-12;
76 diode.C3(diode_i)=52e-12;
```

B.5 Magnetic device general loss model (lib_mag.m)

```
1 %Calculation of core and copper losses in mag devices
2 %Core loss MSE + temp. + dc-bias
3 %INPUT PARAMETERS FROM CONVERTER FILE
4 mag_fs; %Hz
5 mag_feq; %Hz
6 mag_deltaB; %T
7 mag_Bdc; %T
8 mag_mat; %-
9 mag_core; %-
10 mag_Rdc; %ohm
11 mag_FR; %-
12 mag_I; %A
13 mag_Iac; %A
14 mag_T; %deg C
15
16 %INPUT PARAMETERS FROM DATA FILE
17 mag_kfs=1;
18 %Frequency range selection
19 while mag_fs>magmat.fs(mag_kfs,mag_mat)
20 mag_kfs=mag_kfs+1;
21 end
22 mag_k=magmat.k(mag_kfs,mag_mat);
23 mag_alpha=magmat.alpha(mag_kfs,mag_mat);
24 mag_beta=magmat.beta(mag_kfs,mag_mat);
25
26 mag_K1=magmat.K1(mag_kfs,mag_mat);
27 mag_K2=magmat.K2(mag_kfs,mag_mat);
28
29 mag_ct=magmat.ct(mag_kfs,mag_mat);
30 mag_ct1=magmat.ct1(mag_kfs,mag_mat);
31 mag_ct2=magmat.ct2(mag_kfs,mag_mat);
32
33 mag_volume=magcore.volume(mag_core); %cm3
34
```

```

35 %Core loss calculation
36 mag_kprim=mag_k*(1+mag_K1*mag_Bdc*exp(-mag_deltaB/mag_K2)); %dc
    bias coefficient
37 mag_ktemp=mag_ct2*mag_T-mag_ct1*mag_T+mag_ct; %temperature
    coefficient
38 mag_Pfevol=mag_kprim*mag_ktemp*(mag_fs/1e3)*(mag_feq/1e3)^(mag_alp
    ha-1)*(mag_deltaB*10)^mag_beta/1e3; %loss per volume unit
39 mag_Pfe=mag_Pfevol*mag_volume;
40
41 %Copper loss
42 for mag_i=1:size(mag_Rdc,2)
43     mag_Pcudc(mag_i)=mag_Rdc(mag_i)*mag_I(mag_i)^2;
44     mag_Pcuac(mag_i)=mag_FR(mag_i)*mag_Rdc(mag_i)*mag_Iac(mag_i)^2;
45 end

```

B.6 Magnetic core library (data_magcore.m)

```

1 %Core database
2 magcore_i=1;
3 magcore.model(magcore_i)=(['01.E42/21/20']);
4 magcore.volume(magcore_i)=22.7; %cm3
5 magcore.Ag(magcore_i)=2.44; %cm2
6 magcore.lm(magcore_i)=9.7; %cm
7 magcore.Wamax(magcore_i)=2.55; %cm2
8 magcore.Wa(magcore_i)=1.78; %cm2
9
10 magcore_i=magcore_i+1;
11 magcore.model(magcore_i)=(['01.E42/21/15']);
12 magcore.volume(magcore_i)=17.3; %cm3
13 magcore.Ag(magcore_i)=1.85; %cm2
14 magcore.lm(magcore_i)=9.7; %cm
15 magcore.Wamax(magcore_i)=2.55; %cm2
16 magcore.Wa(magcore_i)=1.78; %cm2

```

B.7 Magnetic material library (data_magmat.m)

```

1 %Ferrite - powder materials database
2 magmat_i=1;
3 magmat.mat(magmat_i)=(['01.ideal ferrite']);
4 magmat.fs(:,magmat_i)= [100e3 500e3 inf inf inf];
5 magmat.k(:,magmat_i)= [0 0 0 0 0];
6 magmat.alpha(:,magmat_i)= [1 1 1 1 1];
7 magmat.beta(:,magmat_i)= [1 1 1 1 1];
8 magmat.K1(:,magmat_i)= [0 0 0 0 0];
9 magmat.K2(:,magmat_i)= [1 1 1 1 1];
10 magmat.ct(:,magmat_i)= [1 1 1 1 1];
11 magmat.ct1(:,magmat_i)= [0 0 0 0 0];
12 magmat.ct2(:,magmat_i)= [0 0 0 0 0];
13
14 magmat_i=2;
15 magmat.mat(magmat_i)=(['02.P material Magnetics']);
16 magmat.fs(:,magmat_i)= [100e3 500e3 inf inf inf];
17 magmat.k(:,magmat_i)= [.158 .0434 7.36e-7 0 0];

```

```
18 magmat.alpha(:,magmat_i)= [1.36 1.63 3.47 1 1];
19 magmat.beta(:,magmat_i)= [2.86 2.62 2.54 1 1];
20 magmat.K1(:,magmat_i)= [0 0 0 0 0];
21 magmat.K2(:,magmat_i)= [1 1 1 1 1];
22 magmat.ct(:,magmat_i)= [1 1 1 1 1];
23 magmat.ct1(:,magmat_i)= [0 0 0 0 0];
24 magmat.ct2(:,magmat_i)= [0 0 0 0 0];
```

B.8 Boost converter main file (main_boost.m)

```
1 close all;
2 clear all;
3
4 run ../lib/data_magmat.m;
5 run ../lib/data_magcore.m
6 run ../lib/data_diode.m;
7 run ../lib/data_trans.m;
8
9 %CONVERTER INPUT DATA
10 conv_Vin=30;
11 conv_Vout=90;
12 conv_fs=50e3;
13 conv_Pout=135;
14 conv_eff=1;
15
16 %TRANSISTOR INPUT DATA
17 transT1_model=1+5;
18 transT1_Tj=50;
19 transT1_VGS=14;
20 transT1_Rgon=18+2;
21 transT1_Rgoff=18+2;
22
23 %DIODE INPUT DATA
24 diodeD1_model=1+3;
25 diodeD1_Tj=50;
26
27 %INDUCTOR INPUT DATA
28 magL1_L1=52e-6;
29 magL1_deltaB=0.065;
30 magL1_Bdc=0;
31 magL1_mat=1+1;
32 magL1_core=1;
33 magL1_T=30;
34 magL1_Rdc=4.9e-3;
35 magL1_FR=85/4.9;
36
37 %Run converter model
38 run ./conv_boost.m
39
40 ('done')
```

B.9 Boost converter model (conv_boost.m)

```

1  clear mag_*;
2  clear trans_*;
3  clear diode_*;
4  clear cap_*;
5
6  %CONVERTER INPUT DATA FROM MAIN FILE
7  conv_Vin;
8  conv_Vout;
9  conv_fs;
10 conv_Pout;
11 conv_eff;
12 magL1_L1;
13
14 %Input power and duty cycle
15 conv_Pin=conv_Pout/conv_eff;
16 conv_D=1-conv_Vin/conv_Vout;
17
18 %Currents in the circuit
19 conv_Iout=conv_Pout/conv_Vout;
20 conv_Iin=conv_Pin/conv_Vin;
21 conv_Iinpp=conv_Vin*conv_D/conv_fs/magL1_L1;
22
23 conv_Iint0p=conv_Iin-conv_Iinpp/2;
24 conv_Iint1m=conv_Iin+conv_Iinpp/2;
25 conv_Iint1p=conv_Iint1m;
26 conv_Iint2m=conv_Iint0p;
27
28 %Time instants
29 conv_t0=0;
30 conv_t1=conv_D/conv_fs;
31 conv_t2=1/conv_fs;
32
33
34 %TRANSISTOR
35 %INPUT DATA FROM MAIN FILE
36 trans_model=transT1_model; %NOTE: trans_model=1 is an ideal
    transistor
37 trans_Tj=transT1_Tj;
38 trans_VGS=transT1_VGS;
39 trans_Rgon=transT1_Rgon;
40 trans_Rgoff=transT1_Rgoff;
41 %CALCULATED TRANSISTOR INPUT DATA
42 trans_fs=conv_fs;
43 trans_Irms=sqrt(conv_D*1/3*(conv_Iint0p^2+conv_Iint0p*conv_Iint1m+
    conv_Iint1m^2));
44 trans_Ion=conv_Iint0p;
45 trans_Ioff=conv_Iint1m;
46 trans_Von=conv_Vout;
47 trans_Voff=conv_Vout;
48 %Library call
49 run ../lib/lib_trans.m
50 %Output data from loss model
51 transT1_PTcond=trans_PTcond;
52 transT1_PTon=trans_PTon;
53 transT1_PToff=trans_PToff;

```

```
54 transT1_PTgate=trans_PTgate;
55
56 %DIODE
57 %INPUT DATA FROM MAIN FILE
58 diode_model=diodeD1_model; %NOTE: diode_model=1 is ideal diode
59 diode_Tj=diodeD1_Tj;
60 %CALCULATED DIODE INPUT DATA
61 diode_I=conv_Iout;
62 diode_Irms=sqrt((1-
    conv_D)*1/3*(conv_Iint1p^2+conv_Iint1p*conv_Iint2m+conv_Iint2m^2))
    ;
63 diode_Ioff=conv_Iint2m;
64 diode_Voff=conv_Vout;
65 diode_fs=conv_fs;
66 %Library call
67 run ../lib/lib_diode.m
68 %Output data from loss model
69 diodeD1_PDcond=diode_PDcond;
70 diodeD1_PDrr=diode_PDrr;
71 diodeD1_PDC=diode_PDC;
72
73 %INDUCTOR
74 %INPUT DATA FROM MAIN FILE
75 mag_deltaB=magL1_deltaB;
76 mag_Bdc=magL1_Bdc;
77 mag_mat=magL1_mat;
78 mag_core=magL1_core;
79 mag_T=magL1_T;
80 mag_Rdc=magL1_Rdc;
81 mag_FR=magL1_FR;
82 %CALCULATED INDUCTOR DATA
83 mag_I=conv_Iin;
84 mag_Iac=conv_Iinpp/2/sqrt(3);
85 mag_fs=conv_fs;
86 mag_feq=2/pi^2*((2*mag_deltaB/2/mag_deltaB)^2/(conv_t1-
    conv_t0)+(2*mag_deltaB/2/mag_deltaB)^2/(conv_t2-conv_t1));
87 %Library call
88 run ../lib/lib_mag.m
89 %Output data from loss model
90 magL1_Pcuac=mag_Pcuac;
91 magL1_Pcudc=mag_Pcudc;
92 magL1_Pfe=mag_Pfe;
```

B.10 Non-isolated push-pull-boost converter main file (main_pushpullboost.m)

```
1 close all;
2 clear all;
3
4 run ../lib/data_magmat.m;
5 run ../lib/data_magcore.m;
6 run ../lib/data_diode.m;
7 run ../lib/data_trans.m;
8
```

```

9      %CONVERTER INPUT DATA
10     conv_Vin=30;
11     conv_Vout=400;
12     conv_fs=50e3;
13     conv_Pout=250;
14     conv_eff=.98;
15
16     %TRANSISTOR INPUT DATA
17     transT1_model=6;
18     transT1_Tj=40;
19     transT1_VGS=14;
20     transT1_Rgon=5+2;
21     transT1_Rgoff=5+2;
22
23     %DIODE INPUT DATA LOW VOLTAGE
24     diodeD1_model=4;
25     diodeD1_Tj=40;
26
27     %DIODE INPUT DATA HIGH VOLTAGE
28     diodeD2_model=3;
29     diodeD2_Tj=40;
30
31     %INDUCTOR INPUT DATA
32     magL1_L1=48.3e-6;
33     magL1_deltaB=0.03;
34     magL1_Bdc=0.27;
35     magL1_mat=1+1;
36     magL1_core=1;
37     magL1_T=30;
38     magL1_Rdc=4.2e-3;
39     magL1_FR=247e-3/magL1_Rdc;
40
41     %TRANSFORMER INPUT DATA
42     magTR_deltaB=0.075;
43     magTR_Bdc=0;
44     magTR_mat=2;
45     magTR_core=1;
46     magTR_T=40;
47     magTR_n=2;
48     magTR_Rdc=[4.5e-3 18e-3];
49     magTR_FR=[4.13e-3 16.8e-3]./magTR_Rdc;
50
51     %RUN CONVERTER MODEL
52     run ./conv_pushpullboost.m;
53
54     ('done')

```

B.11 Non-isolated push-pull-boost converter model (conv_pushpullboost.m)

```

1     clear mag_*;
2     clear trans_*;
3     clear diode_*;
4     clear cap_*;

```

```
5
6  %CONVERTER INPUT DATA FROM MAIN FILE
7  conv_Vin;
8  conv_Vout;
9  conv_fs;
10 conv_Pout;
11 conv_eff;
12 magL1_L1;
13 magTR_n;
14
15 %INPUT POWER AND DUTY CYCLE
16 conv_Pin=conv_Pout/conv_eff;
17 conv_D=1-conv_Vin*(1+magTR_n)/conv_Vout;
18
19 %CURRENTS IN CIRCUIT
20 conv_Iout=conv_Pout/conv_Vout;
21 conv_Iin=conv_Pin/conv_Vin;
22 conv_Iinpp=conv_Vin*(conv_D-0.5)/conv_fs/magL1_L1;
23
24 conv_Iint0=conv_Iin-conv_Iinpp/2;
25 conv_Iint1=conv_Iin+conv_Iinpp/2;
26 conv_Iint2=conv_Iint0;
27 conv_Iint3=conv_Iint1;
28 conv_Iint4=conv_Iint0;
29
30 conv_Inlt0p=conv_Iint0/2;
31 conv_Inlt1m=conv_Iint1/2;
32 conv_Inlt1p=conv_Iint1/2/(1+magTR_n);
33 conv_Inlt2m=conv_Iint2/2/(1+magTR_n);
34 conv_Inlt2p=conv_Iint2/2;
35 conv_Inlt3m=conv_Iint3/2;
36 conv_Inlt3p=conv_Iint3-conv_Iint3/2/(1+magTR_n);
37 conv_Inlt4m=conv_Iint4-conv_Iint4/2/(1+magTR_n);
38
39 conv_In2t1p=(conv_Inlt3p-conv_Inlt1p)/(magTR_n);
40 conv_In2t2m=(conv_Inlt4m-conv_Inlt2m)/(magTR_n);
41
42 conv_unlt01=1/3*(conv_Inlt0p^2+conv_Inlt0p*conv_Inlt1m+conv_Inlt1m
^2);
43 conv_unlt12=1/3*(conv_Inlt1p^2+conv_Inlt1p*conv_Inlt2m+conv_Inlt2m
^2);
44 conv_unlt23=1/3*(conv_Inlt2p^2+conv_Inlt2p*conv_Inlt3m+conv_Inlt3m
^2);
45 conv_unlt34=1/3*(conv_Inlt3p^2+conv_Inlt3p*conv_Inlt4m+conv_Inlt4m
^2);
46
47 conv_un2t12=1/3*(conv_In2t1p^2+conv_In2t1p*conv_In2t2m+conv_In2t2m
^2);
48
49 conv_anlt01=(conv_Inlt0p+conv_Inlt1m)/2;
50 conv_anlt12=(conv_Inlt1p+conv_Inlt2m)/2;
51 conv_anlt23=(conv_Inlt2p+conv_Inlt3m)/2;
52 conv_anlt34=(conv_Inlt3p+conv_Inlt4m)/2;
53
54 conv_an2t12=(conv_In2t1p+conv_In2t2m)/2;
55
56 %TIME INSTANTS
```

```

57 conv_t0=0;
58 conv_t1=(conv_D-0.5)/conv_fs;
59 conv_t2=0.5/conv_fs;
60 conv_t3=(conv_D)/conv_fs;
61 conv_t4=1/conv_fs;
62
63 conv_d01=(conv_t1-conv_t0)/(conv_t4-conv_t0);
64 conv_d12=(conv_t2-conv_t1)/(conv_t4-conv_t0);
65 conv_d23=(conv_t3-conv_t2)/(conv_t4-conv_t0);
66 conv_d34=(conv_t4-conv_t3)/(conv_t4-conv_t0);
67
68 %TRANSISTOR
69 %INPUT DATA FROM MAIN FILE
70 trans_model=transT1_model;
71 trans_Tj=transT1_Tj;
72 trans_VGS=transT1_VGS;
73 trans_Rgon=transT1_Rgon;
74 trans_Rgoff=transT1_Rgoff;
75 %CALCULATED TRANSISTOR INPUT DATA
76 trans_fs=conv_fs;
77 trans_Irms=sqrt(conv_d01*conv_unlt01+conv_d23*conv_unlt23+conv_d34
    *conv_unlt34);
78 trans_Ion=conv_Inlt2p;
79 trans_Ioff=conv_Inlt1m;
80 trans_Von=conv_Vout/(1+magTR_n);
81 trans_Voff=conv_Vout/(1+magTR_n);
82 %LIBRARY CALL
83 run ../lib/lib_trans.m;
84 %OUTPUT DATA FROM LOSS MODEL
85 transT1_PTcond=trans_PTcond;
86 transT1_PTon=trans_PTon;
87 transT1_PToff=trans_PToff;
88 transT1_PTgate=trans_PTgate;
89
90 %DIODE LOW VOLTAGE
91 %INPUT DATA FROM MAIN FILE
92 diode_model=diodeD1_model;
93 diode_Tj=diodeD1_Tj;
94 %CALCULATED DIODE INPUT DATA
95 diode_I=conv_d12*conv_anlt12;
96 diode_Irms=sqrt(conv_d12*conv_unlt12);
97 diode_Ioff=conv_Inlt2m;
98 diode_Voff=conv_Vout/(1+magTR_n);
99 diode_fs=conv_fs;
100 %LIBRARY CALL
101 run ../lib/lib_diode.m;
102 %OUTPUT DATA FROM LOSS MODEL
103 diodeD1_PDcond=diode_PDcond;
104 diodeD1_PDrr=diode_PDrr;
105 diodeD1_PDC=diode_PDC;
106
107 %DIODE HIGH VOLTAGE
108 %INPUT DATA FROM MAIN FILE
109 diode_model=diodeD2_model;
110 diode_Tj=diodeD2_Tj;
111 %CALCULATED DIODE INPUT DATA
112 diode_I=conv_d12*conv_an2t12;
113 diode_Irms=sqrt(conv_d12*conv_un2t12);

```

```
114 diode_Ioff=conv_Inlt2m;
115 diode_Voff=conv_Vout*2/(1+magTR_n);
116 diode_fs=conv_fs;
117 %LIBRARY CALL
118 run ../lib/lib_diode.m;
119 %OUTPUT DATA FROM LOSS MODEL
120 diodeD2_PDcond=diode_PDcond;
121 diodeD2_PDrr=diode_PDrr;
122 diodeD2_PDC=diode_PDC;
123
124 %INDUCTOR
125 %INPUT DATA FROM MAIN FILE
126 mag_deltaB=magL1_deltaB;
127 mag_Bdc=magL1_Bdc;
128 mag_mat=magL1_mat;
129 mag_core=magL1_core;
130 mag_T=magL1_T;
131 mag_Rdc=magL1_Rdc;
132 mag_FR=magL1_FR;
133 %CALCULATED INDUCTOR INPUT DATA
134 mag_I=conv_Iin;
135 mag_Iac=conv_Iinpp/2/sqrt(3);
136 mag_fs=conv_fs*2;
137 mag_feq=2/pi^2*(1/(conv_t1-conv_t0)+1/(conv_t2-conv_t1));
138 %LIBRARY CALL
139 run ../lib/lib_mag.m;
140 %OUTPUT DATA FROM LOSS MODEL
141 magL1_Pcuac=mag_Pcuac;
142 magL1_Pcudc=mag_Pcudc;
143 magL1_Pfe=mag_Pfe;
144
145 %TRANSFORMER
146 %INPUT DATA FROM MAIN FILE
147 mag_deltaB=magTR_deltaB;
148 mag_Bdc=magTR_Bdc;
149 mag_mat=magTR_mat;
150 mag_core=magTR_core;
151 mag_T=magTR_T;
152 mag_Rdc=magTR_Rdc;
153 mag_FR=magTR_FR;
154 %CALCULATED INPUT DATA
155 mag_I=[conv_Iin/2 0];
156 mag_Iac=[sqrt(conv_d01*conv_unlt01+conv_d12*conv_unlt12+conv_d23*c
onv_unlt23+conv_d34*conv_unlt34-(conv_Iin/2)^2)
sqrt(2*conv_d12*conv_un2t12)];
157 mag_fs=conv_fs;
158 mag_feq=2/pi^2*(1/(conv_t2-conv_t1)+1/(conv_t4-conv_t3));
159 %LIBRARY CALL
160 run ../lib/lib_mag.m;
161 %OUTPUT DATA FROM LOSS MODEL
162 magTR_Pcuac=mag_Pcuac;
163 magTR_Pcudc=mag_Pcudc;
164 magTR_Pfe=mag_Pfe;
```

B.12 C-code used in the microcontroller

```

1  /* Modulator - phase shifted PWM signal generator by
   pak@iet.aau.dk */
2  #define USE_PEC
3
4  #include <xc161.h>
5  #include <stdio.h>
6  #include <intrins.h>
7  // #include <math.h>
8
9  #define CPU_CLK ((unsigned long) 20000000)
10
11 #pragma PECDEF(7)
12 #pragma PECDEF(6)
13 #pragma PECDEF(5)
14 #pragma PECDEF(4)
15 #pragma PECDEF(3)
16
17 // Macros useful for dealing with Interrupt and PEC registers
18 #define IC_IE(x) ((x) == 0) ? 0x0000 : 0x0040
19 #define IC_ILVL(x) ((x) << 2) & 0x003C
20 #define IC_GLVL(x) ((x) & 0x0003)
21 #define IC_PEC(x) (((x) & 0x0007) | 0x0038)
22
23 unsigned long f;
24 unsigned int i, n, step, ticks, duty_tmp, rel_tmp;
25 unsigned int bdata reload[1];
26 unsigned int bdata duty[1];
27 unsigned int bdata ooff[1];
28 unsigned int chrefon[9], chrefoff[9];
29
30
31 void channel_inc (void) interrupt CC1_CC4=20 {
32     if (n<8) {
33         n=n+1;
34         rel_tmp = 0xFFFF - ((unsigned long) (CPU_CLK/f));
35         ticks=(0xFFFF-rel_tmp);
36         reload[0]=rel_tmp;
37         step=ticks/n;
38         i=0;
39         while (i<n){
40             chrefon[i]=0xFFFF-i*step-step/2;
41             chrefoff[i]=chrefon[i];
42             i++;
43         }
44         i=n;
45         while (i<9){
46             chrefon[i]=0x0;
47             chrefoff[i]=rel_tmp+ticks/2; // turn-off impulses
48             i++;
49         }
50
51         CC1_CC11=chrefon[0]; //P2.11
52         CC1_CC10=chrefon[1]; //P2.10
53         CC1_CC9=chrefon[2]; //P2.9
54         CC1_CC8=chrefon[3]; //P2.8

```

```
55
56     CC1_CC12=chrefon[4]; //P2.12
57     CC1_CC13=chrefon[5]; //P2.13
58     CC1_CC14=chrefon[6]; //P2.14
59     CC1_CC15=chrefon[7]; //P2.15
60
61     CC2_CC18=chrefoff[0]; //P9.2
62     CC2_CC17=chrefoff[1]; //P9.1
63     CC2_CC16=chrefoff[2]; //P9.0
64     CC2_CC19=chrefoff[3]; //P9.3
65
66     CC2_CC20=chrefoff[4]; //P9.4
67     CC2_CC21=chrefoff[5]; //P9.5
68     CC2_CC28=chrefoff[6]; //P7.4
69     CC2_CC29=chrefoff[7]; //P7.5
70 }
71 }
72
73
74 void channel_dec (void) interrupt CC1_CC5=21 {
75     if (n>0) {
76         n=n-1;
77         rel_tmp = 0xFFFF - ((unsigned long) (CPU_CLK/f));
78         ticks=(0xFFFF-rel_tmp);
79         reload[0]=rel_tmp;
80         step=ticks/n;
81         i=0;
82         while (i<n){
83             chrefon[i]=0xFFFF-i*step-step/2;
84             chrefoff[i]=chrefon[i];
85             i++;
86         }
87         i=n;
88         while (i<9){
89             chrefon[i]=0x0;
90             chrefoff[i]=rel_tmp+ticks/2; // turn-off impulses
are always available
91             i++;
92         }
93
94     CC1_CC11=chrefon[0]; //P2.11
95     CC1_CC10=chrefon[1]; //P2.10
96     CC1_CC9=chrefon[2]; //P2.9
97     CC1_CC8=chrefon[3]; //P2.8
98
99     CC1_CC12=chrefon[4]; //P2.12
100    CC1_CC13=chrefon[5]; //P2.13
101    CC1_CC14=chrefon[6]; //P2.14
102    CC1_CC15=chrefon[7]; //P2.15
103
104    CC2_CC18=chrefoff[0]; //P9.2
105    CC2_CC17=chrefoff[1]; //P9.1
106    CC2_CC16=chrefoff[2]; //P9.0
107    CC2_CC19=chrefoff[3]; //P9.3
108
109    CC2_CC20=chrefoff[4]; //P9.4
110    CC2_CC21=chrefoff[5]; //P9.5
111    CC2_CC28=chrefoff[6]; //P7.4
112    CC2_CC29=chrefoff[7]; //P7.5
```

```

113     }
114     if (n==0) { // decrease gain when all modules are down -
avoid inrush current when modules turn-on again
115         //gain=11;
116         duty[0]=reload[0]+1;
117     }
118 }
119
120 void pwm_inc (void) interrupt CC2_CC30=69 {
121     if (n>0){
122         if (duty[0]<0xFFFFA) {
123             if (duty[0]<(reload[0]+ticks/2))
124                 duty_tmp=duty[0]+3 ;
125             else
126                 duty_tmp=duty[0]+1;
127             duty[0]=duty_tmp;
128         }
129     }
130     else if (n==0 & f<60000){
131         f = f + 1000;
132         reload[0]=0xFFFF-((unsigned long) (CPU_CLK/f));
133         ticks=(0xFFFF-reload[0]);
134         CC1_T0REL=reload[0];
135         CC2_T7REL=reload[0]+36;
136         CC2_CC18=reload[0]+ticks/2; //P9.2
137         CC2_CC17=reload[0]+ticks/2; //P9.1
138         CC2_CC16=reload[0]+ticks/2; //P9.0
139         CC2_CC19=reload[0]+ticks/2; //P9.3
140         CC2_CC20=reload[0]+ticks/2; //P9.4
141         CC2_CC21=reload[0]+ticks/2; //P9.5
142         CC2_CC28=reload[0]+ticks/2; //P7.4
143         CC2_CC29=reload[0]+ticks/2; //P7.5
144     }
145 }
146 }
147
148 void pwm_dec (void) interrupt CC2_CC31=70 {
149     if (n>0){
150         if (duty[0]>reload[0]+1) {
151             if (duty[0]<(reload[0]+ticks/2))
152                 duty_tmp=duty[0]-3 ;
153             else
154                 duty_tmp=duty[0]-1;
155             duty[0]=duty_tmp;
156         }
157     }
158     else if (n==0 & f>20000){
159         f = f - 1000;
160         reload[0]=0xFFFF-((unsigned long) (CPU_CLK/f));
161         ticks=(0xFFFF-reload[0]);
162         CC1_T0REL=reload[0];
163         CC2_T7REL=reload[0]+36;
164         CC2_CC18=reload[0]+ticks/2; //P9.2
165         CC2_CC17=reload[0]+ticks/2; //P9.1
166         CC2_CC16=reload[0]+ticks/2; //P9.0
167         CC2_CC19=reload[0]+ticks/2; //P9.3
168         CC2_CC20=reload[0]+ticks/2; //P9.4
169         CC2_CC21=reload[0]+ticks/2; //P9.5
170         CC2_CC28=reload[0]+ticks/2; //P7.4

```

```
171         CC2_CC29=reload[0]+ticks/2; //P7.5
172     }
173 }
174
175 //void adc_to_duty (void) interrupt ADC_IC=40 {
176 //    duty_tmp=reload[0] + ((double) ((ADC_DAT & 0x00FF) +
177 //    256)/512)*ticks;
178 //    duty[0]=duty_tmp;
179 //}
180
181 //void frequency_setup (unsigned int rel){
182 //}
183
184 //void serial_setup (void){
185 //    DP3 |= 0x400;
186 //    DP3 &= ~0x0800;
187 //    P3 |= 0x0400;
188 //    S0BG = 0x0040;
189 //    S0CON = 0x8011;
190
191 //    S0TBUF = 0x0040;
192 //    S0RBUF = 0x000F;
193 //}
194 //*****
195 void main (void) {
196     // Port direction and output type setup
197     DP2=0xFF00;
198     ODP2=0x0000; //push pull outputs
199     ALTSEL0P2=0xFF00; // alternate function of P2 - required in
200     non-staggered mode od CAPCOM1
201     POC0N2=0x4400; // output driver control strong driver soft
202     edge
203
204     DP9=0x00FF;
205     ALTSEL1P9=0x00FF;
206     //POCON9=0x0044; // output driver control strong driver soft
207     edge
208
209     DP7=0x0030;
210     ALTSEL1P7=0x0030;
211     //POCON7=0x0040; // output driver control strong driver soft
212     edge
213
214     //PICON=0x0060; // 0x0060 - use cmos treshold on ports P6 &
215     P7
216
217     // Frequency f=(305Hz-20MHz) @ 20MHz
218     f=30000;
219     reload[0]=0xFFFF-((unsigned long) (CPU_CLK/f)); //
220     initial value
221     ticks=(0xFFFF-reload[0]); //initial value
222
223     // A-D conversion setup
224     //P5DIDIS_P0=1; // pin as AD converter input, alternate
225     function
226     //ADC_CON=0xF210; //0xB210
227     //ADC_CON1=0x1000; // 1000 - 8-bit resolution
```



```

221
222     // CAPCOM  setup
223
224     CC1_T0REL=reload[0];
225     CC2_T7REL=reload[0]+36;
226
227     CC1_T01CON=0x0000; //0x0707;
228     CC1_IOC=0x0004; //0x0004 non-staggered mode -
CC_clock=CPU_CLK
229
230     CC1_M0=0x0004; // 0x7 - T0/T7 Compare Mode 3 (one event /
period, IRQ + pin)
231     CC1_M1=0x0011; // 0x4 - T0/T7 Compare Mode 0 (many events /
period, IRQ only)
232     CC1_M2=0x7777; // 0x1 - T0/T7 Capture Mode, Rising Edge; 0x2
- T0/T7 Capture Mode, Falling Edge;
233     CC1_M3=0x7777; //
234
235     CC2_T78CON=CC1_T01CON; // the same settings like T0 & T1
236     CC2_IOC=CC1_IOC; //      the same settings like T0 & T1
237
238     CC2_M4=0x7777;
239     CC2_M5=0x0077;
240     CC2_M6=0x0000;
241     CC2_M7=0x1177;
242
243     CC2_CC18=reload[0]+ticks/2; //P9.2
244     CC2_CC17=reload[0]+ticks/2; //P9.1
245     CC2_CC16=reload[0]+ticks/2; //P9.0
246     CC2_CC19=reload[0]+ticks/2; //P9.3
247
248     CC2_CC20=reload[0]+ticks/2; //P9.4
249     CC2_CC21=reload[0]+ticks/2; //P9.5
250     CC2_CC28=reload[0]+ticks/2; //P7.4
251     CC2_CC29=reload[0]+ticks/2; //P7.5
252
253     // Interrupts and PEC setup
254     CC1_CC0IC=IC_IE(1)|IC_PEC(7); // Reload T7 on "duty" compare
event in CC0
255     PECC7 = 0x00FF;
256     DSTP7 = (unsigned int) &CC2_T7;
257     SRCP7 = _sof_ (reload);
258
259     CC1_T0IC=IC_IE(1)|IC_PEC(5); // Reload duty ratio CC0 on T0
overflow
260     PECC5 = 0x00FF;
261     DSTP5 = (unsigned int) &CC1_CC0;
262     SRCP5 = _sof_ (duty);
263
264     CC1_CC4IC=IC_IE(1)|IC_ILVL(12)|IC_GLVL(0); // Active
channels increase P6.4
265     CC1_CC5IC=IC_IE(1)|IC_ILVL(12)|IC_GLVL(1); // Active
channels decrease P6.5
266
267     CC2_CC30IC=IC_IE(1)|IC_ILVL(12)|IC_GLVL(2); // PWM increase
P7.6
268     CC2_CC31IC=IC_IE(1)|IC_ILVL(12)|IC_GLVL(3); // PWM decrease
P7.7
269

```

```
270      // Global interrupt enable
271      PSW_IEN=1;
272
273      // Peripherals run
274      CC2_T78CON_T7R=1;
275      CC1_T01CON_T0R=1;
276
277      // Initial variable values
278      n=0; //initial number of active channels
279      duty[0]=reload[0]+1;
280      while(1){
281
282      };
283 }
```

Bibliography

- [1] Z. Fu and W. Qu, "Implementation of a current share method for paralleling of DC/DC converter without control interconnection," in *Electrical Machines and Systems, 2003. ICEMS 2003. Sixth International Conference on*, 2003, pp. 394-397 vol.1.
- [2] P. Klimczak and P. Munk-Nielsen, "A single switch dual output non-isolated boost converter," in *Applied Power Electronics Conference and Exposition, 2008. APEC 2008. Twenty-Third Annual IEEE*, 2008, pp. 43-47.
- [3] G. Hoogers, *Fuel cell technology handbook* CRC Press, 2003.
- [4] W. Vielstich, A. Lamm, and H. A. Gasteiger, *Handbook of fuel cells fundamentals, technology, and applications*: Wiley, 2003.
- [5] W. Rong-Jong and D. Rou-Yong, "High step-up converter with coupled-inductor," *Power Electronics, IEEE Transactions on*, vol. 20, pp. 1025-1035, 2005.
- [6] P. Zacharias, B. Sahan, S. V. Araújo, F. L. M. Antunes, and R. T. Bascopé, "Analysis and Proposition of a PV Module Integrated Converter with High Voltage Gain Capability in a non-isolated Topology," in *The 7th International Conference on Power Electronics* Daegu, Korea: IEEE, 2007.
- [7] O. B. Cruz and L. D. Olavarrieta, "A Bird's Eye View of Materials and Manufacturing Processes for Photovoltaic Cells," in *Electronics, Communications and Computers, 2005. CONIELECOMP 2005. Proceedings. 15th International Conference on*, 2005, pp. 251-256.
- [8] A. Goetzberger and V. U. Hoffmann, *Photovoltaic solar energy generation*: Springer, 2005.
- [9] "Global Market Outlook Until 2013," in http://www.epia.org/fileadmin/EPIA_docs/publications/epia/Global_Market_Outlook_Until_2013.pdf: European Photovoltaic Industry Association, 2009.
- [10] T. Kerekes, R. Teodorescu, and U. Borup, "Transformerless Photovoltaic Inverters Connected to the Grid," in *Applied Power Electronics Conference, APEC 2007 - Twenty Second Annual IEEE*, 2007, pp. 1733-1737.
- [11] H. Patel and V. Agarwal, "A Single-Stage Single-Phase Transformer-Less Doubly Grounded Grid-Connected PV Interface," *Energy conversion, iee transactions on*, vol. 24, pp. 93-101, 2009.
- [12] "IEEE guide for terrestrial photovoltaic power system safety," *IEEE Std 1374-1998*, 1998.
- [13] W. Vielstich, *Handbook of fuel cells fundamentals, technology, and applications editors*, Wolf Vielstich, Arnold Lamm, Hubert A. Gasteiger: Wiley, 2003.

- [14] Y. Kanthaphayao and C. Boonmee, "Dual-output DC-DC power supply without transformer," in *TENCON 2004. 2004 IEEE Region 10 Conference*, 2004, pp. 41-44 Vol. 4.
- [15] P. Klimczak and S. Munk-Nielsen, "A single switch dual output non-isolated boost converter," in *Applied Power Electronics Conference and Exposition, 2008. APEC 2008. Twenty-Third Annual IEEE*, 2008, pp. 43-47.
- [16] F. L. Luo, "Double-output Luo converters, an advanced voltage-lift technique," *Electric Power Applications, IEE Proceedings -*, vol. 147, pp. 469-485, 2000.
- [17] O. Won-Sik, H. Sang-Kyoo, C. Seong-Wook, and M. Gun-Woo, "Three phase three-level PWM switched voltage source inverter with zero neutral point potential," in *Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual*, 2004, pp. 4405-4410 Vol.6.
- [18] Z. Qun and F. C. Lee, "High-efficiency, high step-up DC-DC converters," *Power Electronics, IEEE Transactions on*, vol. 18, pp. 65-73, 2003.
- [19] K. C. Tseng and T. J. Liang, "Novel high-efficiency step-up converter," *Electric Power Applications, IEE Proceedings -*, vol. 151, pp. 182-190, 2004.
- [20] H. Shu-Hung Chung, "Design and analysis of a switched-capacitor-based step-up DC/DC converter with continuous input current," *Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on [see also Circuits and Systems I: Regular Papers, IEEE Transactions on]*, vol. 46, pp. 722-730, 1999.
- [21] M. On-Cheong, W. Yue-Chung, and A. Ioinovici, "Step-up DC power supply based on a switched-capacitor circuit," *Industrial Electronics, IEEE Transactions on*, vol. 42, pp. 90-97, 1995.
- [22] O. Abutbul, A. Gherlitz, Y. Berkovich, and A. Ioinovici, "Step-up switching-mode converter with high voltage gain using a switched-capacitor circuit," *Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on [see also Circuits and Systems I: Regular Papers, IEEE Transactions on]*, vol. 50, pp. 1098-1102, 2003.
- [23] K. K. Law, K. W. E. Cheng, and Y. P. B. Yeung, "Design and analysis of switched-capacitor-based step-up resonant converters," *Circuits and Systems I: Regular Papers, IEEE Transactions on [Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on]*, vol. 52, pp. 943-948, 2005.
- [24] D. A. Grant and Y. Darroman, "Extending the tapped-inductor DC-to-DC converter family," *Electronics Letters*, vol. 37, pp. 145-146, 2001.
- [25] Z. Qun, T. Fengfeng, and F. C. Lee, "A front-end DC/DC converter for network server applications," in *Power Electronics Specialists Conference, 2001. PESC. 2001 IEEE 32nd Annual*, 2001, pp. 1535-1539 vol. 3.
- [26] C. E. A. Silva, R. P. T. Bascope, and D. S. Oliveira, "Proposal of a New High Step-Up Converter for UPS Applications," in *Industrial Electronics, 2006 IEEE International Symposium on*, 2006, pp. 1288-1292.
- [27] D. M. Van de Sype, K. De Gussemé, B. Renders, A. R. Van den Bossche, and J. A. Melkebeek, "A single switch boost converter with a high conversion ratio," in *Applied Power Electronics Conference and Exposition, 2005. APEC 2005. Twentieth Annual IEEE*, 2005, pp. 1581-1587 Vol. 3.

-
- [28] R. J. Wai and R. Y. Duan, "High-efficiency DC/DC converter with high voltage gain," *Electric Power Applications, IEE Proceedings -*, vol. 152, pp. 793-802, 2005.
 - [29] B. Ju-Won, R. Myung-Hyo, K. Tae-Jin, Y. Dong-Wook, and K. Jong-Soo, "High boost converter using voltage multiplier," in *Industrial Electronics Society, 2005. IECON 2005. 31st Annual Conference of IEEE*, 2005, p. 6 pp.
 - [30] L. C. Franco, L. L. Pfitscher, and R. Gules, "A new high static gain nonisolated DC-DC converter," in *Power Electronics Specialist Conference, 2003. PESC '03. 2003 IEEE 34th Annual*, 2003, pp. 1367-1372 vol.3.
 - [31] G. V. Torrico-Bascope, R. P. Torrico-Bascope, D. S. Oliviera, F. L. M. Antunes, S. V. Araujo, and C. G. C. Branco, "A Generalized High Voltage Gain Boost Converter Based on Three-State Switching Cell," in *The 32nd Annual Conference of the IEEE Industrial Electronics Society IECON'06*, Paris, France, 2006, pp. 1927-1932.
 - [32] L. Fang Lin, "Luo-Converters, a series of new DC-DC step-up (boost) conversion circuits," in *Power Electronics and Drive Systems, 1997. Proceedings., 1997 International Conference on*, 1997, pp. 882-888 vol.2.
 - [33] F. L. Luo, "Negative output Luo converters: voltage lift technique," *Electric Power Applications, IEE Proceedings -*, vol. 146, pp. 208-224, 1999.
 - [34] F. L. Luo, "Positive output Luo converters: voltage lift technique," *Electric Power Applications, IEE Proceedings -*, vol. 146, pp. 415-432, 1999.
 - [35] F. L. Y. H. Luo, *Advanced DC/DC converters*. Boca Raton: CRC Press, 2004.
 - [36] B. Farhangi and S. Farhangi, "Comparison of z-source and boost-buck inverter topologies as a single phase transformer-less photovoltaic grid-connected power conditioner," in *Power Electronics Specialists Conference, 2006. PESC '06. 37th IEEE*, 2006, pp. 1-6.
 - [37] L. Poh Chiang, D. M. Vilathgamuwa, Y. S. Lai, C. Geok Tin, and Y. Li, "Pulse-width modulation of Z-source inverters," *Power Electronics, IEEE Transactions on*, vol. 20, pp. 1346-1355, 2005.
 - [38] L. Shiguo, Y. Zhihong, L. Ray-Lee, and F. C. Lee, "A classification and evaluation of paralleling methods for power supply modules," in *Power Electronics Specialists Conference, 1999. PESC 99. 30th Annual IEEE*, 1999, pp. 901-908 vol.2.
 - [39] L. Po-Wa, L. Yim-Shu, D. K. W. Cheng, and L. Xiu-Cheng, "Steady-state analysis of an interleaved boost converter with coupled inductors," *Industrial Electronics, IEEE Transactions on*, vol. 47, pp. 787-795, 2000.
 - [40] W. Wei and L. Yim-Shu, "A two-channel interleaved boost converter with reduced core loss and copper loss," in *Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual*, 2004, pp. 1003-1009 Vol.2.
 - [41] "Ferroxcube Product Selection Guide," in <http://www.ferroxcube.com/appl/info/PSG2003.pdf>, 2003.
 - [42] P. Klimczak and S. Munk-Nielsen, "Comparative study on paralleled vs. scaled dc-dc converters in high voltage gain applications," in *Power Electronics and Motion Control Conference, 2008. EPE-PEMC 2008. 13th*, 2008, pp. 108-113.

- [43] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power electronics : converters, applications, and design*, 3rd ed.: John Wiley & Sons, 2003.
- [44] G. V. T. Bascope and I. Barbi, "Generation of a family of non-isolated DC-DC PWM converters using new three-state switching cells," in *Power Electronics Specialists Conference, 2000. PESC 00. 2000 IEEE 31st Annual*, 2000, pp. 858-863 vol.2.
- [45] H. Kragh, *Modeling, Analysis and Optimisation of Power Electronic Circuits for Low-Cost Drives*, PhD thesis, Aalborg University, 2000
- [46] I. Budihardjo, P. O. Lauritzen, K. Y. Wong, R. B. Darling, and H. A. Mantooth, "Defining standard performance levels for power semiconductor devices," in *Industry Applications Conference, 1995. Thirtieth IAS Annual Meeting, IAS '95., Conference Record of the 1995 IEEE*, 1995, pp. 1084-1090 vol.2.
- [47] R. W. Erickson and D. Maksimovic, *Fundamentals of power electronics*, 2nd ed. Norwell, Mass.: Kluwer Academic, 2001.
- [48] J. Brown, "Modeling the switching performance of a MOSFET in the high side of a non-isolated buck converter," *Power Electronics, IEEE Transactions on*, vol. 21, pp. 3-10, 2006.
- [49] Z. J. Shen, X. Yali, C. Xu, F. Yue, and P. Kumar, "Power MOSFET Switching Loss Analysis: A New Insight," in *Industry Applications Conference, 2006. 41st IAS Annual Meeting. Conference Record of the 2006 IEEE*, 2006, pp. 1438-1442.
- [50] J. Waite and T. G. Wilson, Jr., "Use of simulation to understand and predict switching losses in a two-stage power factor corrected AC-to-DC converter," in *Applied Power Electronics Conference and Exposition, 1996. APEC '96. Conference Proceedings 1996., Eleventh Annual*, 1996, pp. 88-95 vol.1.
- [51] C. L. Ma and P. O. Lauritzen, "A simple power diode model with forward and reverse recovery," *Power Electronics, IEEE Transactions on*, vol. 8, pp. 342-346, 1993.
- [52] S. P. Pendharkar, M. Trivedi, and K. Shenai, "Dynamics of reverse recovery of high-power P-i-N diodes," *Electron Devices, IEEE Transactions on*, vol. 43, pp. 142-149, 1996.
- [53] R. Burkel and T. Schneider, "Fast Recovery Epitaxial Diodes (FRED) Characteristics - Applications - Examples," in http://www.ixyspower.com/images/technical_support/Application%20Notes%20By%20Topic/FREDs,%20Schottky%20and%20GaAS%20Diodes/IXAN0044.pdf, I. P. A. Note, Ed., 1999.
- [54] S. L. M. Berleze and R. Robert, "Skin and proximity effects in nonmagnetic conductors," *Education, IEEE Transactions on*, vol. 46, pp. 368-372, 2003.
- [55] K. W. Klontz, "Skin and proximity effects in multi-layer transformer windings of finite thickness," in *Industry Applications Conference, 1995. Thirtieth IAS Annual Meeting, IAS '95., Conference Record of the 1995 IEEE*, 1995, pp. 851-858 vol.1.
- [56] J. D. Pollock and C. R. Sullivan, "Modelling Foil Winding Configurations with Low AC and DC Resistance," in *Power Electronics Specialists Conference, 2005. PESC '05. IEEE 36th*, 2005, pp. 1507-1512.

-
- [57] A. Reatti and M. K. Kazimierczuk, "Comparison of various methods for calculating the AC resistance of inductors," *Magnetics, IEEE Transactions on*, vol. 38, pp. 1512-1518, 2002.
 - [58] A. M. Urling, V. A. Niemela, G. R. Skutt, and T. G. Wilson, "Characterizing high-frequency effects in transformer windings-a guide to several significant articles," in *Applied Power Electronics Conference and Exposition, 1989. APEC' 89. Conference Proceedings 1989., Fourth Annual IEEE*, 1989, pp. 373-385.
 - [59] J. P. Vandelac and P. D. Ziogas, "A novel approach for minimizing high-frequency transformer copper losses," *Power Electronics, IEEE Transactions on*, vol. 3, pp. 266-277, 1988.
 - [60] N. Xi and C. R. Sullivan, "An improved calculation of proximity-effect loss in high-frequency windings of round conductors," in *Power Electronics Specialist Conference, 2003. PESC '03. 2003 IEEE 34th Annual*, 2003, pp. 853-860 vol.2.
 - [61] J. D. Pollock and C. R. Sullivan, "Gapped-inductor foil windings with low AC and DC resistance," in *Industry Applications Conference, 2004. 39th IAS Annual Meeting. Conference Record of the 2004 IEEE*, 2004, p. 557.
 - [62] F. Robert, P. Mathys, and J. P. Schauwers, "Ohmic losses calculation in SMPS transformers: numerical study of Dowell's approach accuracy," *Magnetics, IEEE Transactions on*, vol. 34, pp. 1255-1257, 1998.
 - [63] J. Reinert, A. Brockmeyer, and R. W. A. A. De Doncker, "Calculation of losses in ferro- and ferrimagnetic materials based on the modified Steinmetz equation," *Industry Applications, IEEE Transactions on*, vol. 37, pp. 1055-1061, 2001.
 - [64] C. D. Graham, "Physical origin of losses in conducting ferromagnetic materials (invited)." vol. 53: AIP, 1982, pp. 8276-8280.
 - [65] M. Albach, T. Durbaum, and A. Brockmeyer, "Calculating core losses in transformers for arbitrary magnetizing currents a comparison of different approaches," in *Power Electronics Specialists Conference, 1996. PESC '96 Record., 27th Annual IEEE*, 1996, pp. 1463-1468 vol.2.
 - [66] L. Jieli, T. Abdallah, and C. R. Sullivan, "Improved calculation of core loss with nonsinusoidal waveforms," in *Industry Applications Conference, 2001. Thirty-Sixth IAS Annual Meeting. Conference Record of the 2001 IEEE*, 2001, pp. 2203-2210 vol.4.
 - [67] A. Van den Bossche, V. C. Valchev, and G. B. Georgiev, "Measurement and loss model of ferrites with non-sinusoidal waveforms," in *Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual*, 2004, pp. 4814-4818 Vol.6.
 - [68] K. Venkatachalam, C. R. Sullivan, T. Abdallah, and H. A. T. H. Tacca, "Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only Steinmetz parameters," in *Computers in Power Electronics, 2002. Proceedings. 2002 IEEE Workshop on*, 2002, pp. 36-41.
 - [69] C. A. Baguley, B. Carsten, and U. K. Madawala, "The Effect of DC Bias Conditions on Ferrite Core Losses," *Magnetics, IEEE Transactions on*, vol. 44, pp. 246-252, 2008.

- [70] A. Brockmeyer, "Experimental evaluation of the influence of DC-premagnetization on the properties of power electronic ferrites," in *Applied Power Electronics Conference and Exposition, 1996. APEC '96. Conference Proceedings 1996., Eleventh Annual, 1996*, pp. 454-460 vol.1.
- [71] W. Hongfang and F. Wang, "Power MOSFETs Paralleling Operation for High Power High Density Converters," in *Industry Applications Conference, 2006. 41st IAS Annual Meeting. Conference Record of the 2006 IEEE, 2006*, pp. 2284-2289.
- [72] Y. Zhai and L. Vu-Quoc, "Analysis of Power Magnetic Components With Nonlinear Static Hysteresis: Proper Orthogonal Decomposition and Model Reduction," *Magnetics, IEEE Transactions on*, vol. 43, pp. 1888-1897, 2007.
- [73] "American National Standard guide on the application and evaluation of EMI power-line filters for commercial use," *ANSI C63.13-1991*, 1991.
- [74] "IEEE standard procedure for measuring conducted emissions in the range of 300 kHz to 25 MHz from television and FM broadcast receivers to power lines," *ANSI/IEEE Std 213-1987*, 1988.
- [75] D. L. Jones, "PCB Design Tutorial," in <http://alternatezone.com/electronics/files/PCBDesignTutorialRevA.pdf>, 2004.
- [76] F. Dong Tan, J. L. Vollin, and S. M. Cuk, "A practical approach for magnetic core-loss characterization," *Power Electronics, IEEE Transactions on*, vol. 10, pp. 124-130, 1995.
- [77] "Farnell," in <http://www.farnell.com>.
- [78] "International Rectifier," in <http://www.irf.com>.
- [79] M. H. Rashid, *Power electronics handbook* Academic Press, 2001.
- [80] "Infineon Technologies," in <http://www.infineon.com>.
- [81] "Magnetics Cores for SMPS," in <http://www.mag-inc.com/pdf/ps-01.pdf>.
- [82] A. V. d. Bossche and V. C. Valchev, *Inductors and transformers for power electronics* CRC Press, 2005
- [83] C. W. T. McLyman, *Transformer and inductor design handbook*: Marcel Dekker, 2004.
- [84] "Magnetics," in <http://www.mag-inc.com>.
- [85] "Ferroxcube," in <http://www.ferroxcube.com>.
- [86] S. Cuk, "New magnetic structures for switching converters," *Magnetics, IEEE Transactions on*, vol. 19, pp. 75-83, 1983.
- [87] C. Rong-Tai and C. Yung-Yaw, "A novel single stage push pull converter with integrated magnetics and ripple-free input current," in *Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual, 2004*, pp. 3848-3853 Vol.5.
- [88] N. Hur and N. Kwanghee, "A robust load-sharing control scheme for parallel-connected multisystems," *Industrial Electronics, IEEE Transactions on*, vol. 47, pp. 871-879, 2000.
- [89] T. Kohama, T. Ninomiya, M. Shoyama, and F. Ihara, "Dynamic analysis of parallel-module converter system with current balance controllers," in

-
- Telecommunications Energy Conference, 1994. INTELEC '94., 16th International, 1994*, pp. 190-195.
- [90] D. J. Perreault, K. Sato, R. L. Selders, Jr., and J. G. Kassakian, "Switching-ripple-based current sharing for paralleled power converters," *Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on* [see also *Circuits and Systems I: Regular Papers, IEEE Transactions on*], vol. 46, pp. 1264-1274, 1999.
 - [91] D. J. Perreault, R. L. Selders, and J. G. Kassakian, "Frequency-based current-sharing techniques for paralleled power converters," in *Power Electronics Specialists Conference, 1996. PESC '96 Record., 27th Annual IEEE, 1996*, pp. 1073-1079 vol.2.
 - [92] H. H. C. Iu and V. Pjevalica, "Experimental study of instabilities in two parallel-connected boost converters under current mode control," in *Power Electronics and Applications, 2005 European Conference on, 2005*, p. 8 pp.
 - [93] S. K. Mazumder, "Stability analysis of parallel DC-DC converters," *Aerospace and Electronic Systems, IEEE Transactions on*, vol. 42, pp. 50-69, 2006.
 - [94] J. M. Zhang, X. G. Xie, X. K. Wu, and Q. Zhaoming, "Stability study for paralleled DC/DC converters," in *Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual, 2004*, pp. 1569-1575 Vol.2.
 - [95] J. G. Kassakian and D. Lau, "An analysis and experimental verification of parasitic oscillations in paralleled power MOSFET's," *Electron Devices, IEEE Transactions on*, vol. 31, pp. 959-963, 1984.
 - [96] P. Wallmeier, "Pre-optimization of linear and nonlinear inductors using area-product formulation," in *Industry Applications Conference, 2002. 37th IAS Annual Meeting. Conference Record of the, 2002*, pp. 2445-2450 vol.4.
 - [97] R. Ayyanar, R. Giri, and N. Mohan, "Active input-voltage and load-current sharing in input-series and output-parallel connected modular DC-DC converters using dynamic input-voltage reference scheme," *Power Electronics, IEEE Transactions on*, vol. 19, pp. 1462-1473, 2004.
 - [98] "TOELLNER Electronic Instrumente GmbH," in http://www.toellner.de/pdf_gb/8871.pdf.
 - [99] "zentro-elektrik GmbH KG " in [http://www.zentro-elektrik.de/inhalte/Elektronische DC Lasten 2007 12 11 20 09 17/ELA 500 EL1000_series.pdf](http://www.zentro-elektrik.de/inhalte/Elektronische_DC_Lasten_2007_12_11_20_09_17/ELA_500_EL1000_series.pdf).
 - [100] "GOOD WILL INSTRUMENT CO., LTD. - GW Instek," in http://www.gwinstek.com/html/en/showproductdetail-e.asp?pd1_sn=120.
 - [101] "Fluke Deutschland GmbH," in http://www.fluke.de/comx/show_product.aspx?locale=dede&pid=35911.
 - [102] "Tektronix, Inc.," in <http://www.tek.com>.
 - [103] "LEM Probes," in <http://www.lem.com>
<http://www.techedu.com/pdf/LEM/PR50.pdf>.
 - [104] M. Nymand and M. A. E. Andersen, "A new approach to high efficiency in isolated boost converters for high-power low-voltage fuel cell applications," in *Power Electronics and Motion Control Conference, 2008. EPE-PEMC 2008. 13th, 2008*, pp. 127-131.

- [105] M. Nymand and M. A. E. Andersen, "New Primary-Parallel Boost Converter for High-Power High-Gain Applications," in *Applied Power Electronics Conference and Exposition, 2009. APEC 2009. Twenty-Fourth Annual IEEE*, 2009, pp. 35-39.